Semiconductor Memories: the follow-up of a successful story

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Organizer

Prof. Francisco Gamiz, Universidad de Granada & REMINDER Project

Abstract

In 1968, Dr.Robert Dennard from IBM introduced the concept of Dynamic Random Access Memory (DRAM) cell, which consists in a transistor (1T) and a capacitor (1C) where the information is stored. Since its introduction almost 50 years ago, this memory cell has been present in all electronic devices up to now. However, the arrival of the Internet of Things (IoT) and the requirement of ultra-low power consumption and extremely cheap devices are making developers to reconsider their design goals, by using memory in new and innovative ways. In many cases, this involves using new, or less familiar, memory technologies and examining memory much earlier in their design cycles. The vast majority of embedded memories are currently charged based (DRAM, FLASH) or flip-flop based (SRAM), the last one penalized by its huge area consumption. The other alternative storage options (which are not yet mature from and commercial perspective) can be grouped into three categories, ReRAM (resistive) or MRAM (magnetic), and body-charged memories (so called floating-body DRAMs, FB-DRAM). All these memory approaches will be analyzed by well-known experts in the field both from Industry and Academia.

Programme

8.30	Welcome Introduction	Prof. Francisco Gamiz (Universidad de Granada, REMINDER project)
9.00	MRAM solutions	Dr. Kilho Lee (title TBC) (MRAM Team, Samsung Electronics, Korea)
9.45	FDX12 technology and embedded NVM solutions for IoT	Dr. Manfrest Horstman (Global Foundries, Dresden, Germany)
10.30	Resistive memories for spike-based neuromorphic circuits	Dr. Elisa Vianello (CEA, France)
11.15	Coffee Break	
11.45	Stand-alone DRAM memory status and challenges	Dr. Pierre Fazan (Micron Europe, Leuven, Belgium)
12.30	MRAM developments at IBM	Dr. Guohan Hu (title TBC) (IBM Yorktown Heights, New York, USA)
13.15	Lunch	
14.30	FDSOI technology for IoT applications	Dr. Philippe Galy (STMicroelectronics)
15.00	Z2FET memory for low-power applications	Prof. Sorin Cristoloveanu (IMEP-MINATEC, Grenoble France)
15.30	Modelling of Z2FET memory cell	Dr. Joris Lacord (CEA-LETI, Grenoble)
16.00	Coffee Break	
16.30	Variability of Z2FET memory cells and matrix	Prof. Asen Asenov (Glasgow and Synopsys U.K.)
17.00	Circuit design with Z2FET memory cell for low-power applications	Dr. Andy Pickering (Surecore U.K.)
17.30	Conclusions	

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