ESSDERC

47th European Solid-State Device Research Conference

September 11-14, 2017
Leuven, Belgium

PROGRAM

IEEE

Electron Devices Society


LEUVEN 2017
ESSDERC
ESSCIRC

September 11-14, 2017
Leuven, Belgium

ESSDERC

47th European Solid-State Device Research Conference

Organized by

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Combining a passion for technology with truly inspired engineering, Melexis designs, develops and delivers innovative micro-electronic solutions that enable designers to turn ideas into applications that support the best imaginable future. The company's advanced mixed-signal semiconductor sensor and actuator components address the challenges of integrating sensing, driving and communication into next-generation products and systems that improve safety, raise efficiency, support sustainability and enhance comfort.

A world leader in automotive semiconductor sensors, Melexis has used its core experience in creating chips for vehicle electronics to expand its portfolio of sensors, driver ICs and wireless devices to also meet the needs of smart appliances, home automation, industrial and medical applications. Melexis sensing solutions include magnetic sensors, MEMS sensors (pressure, TPMS, infrared), sensor interface ICs, optoelectronic single point and linear array sensors and Time of Flight. The company's driver IC portfolio incorporates advanced DC & BLDC motor controllers, LED drivers and FET pre-driver ICs, while Melexis has the know-how and expertise to build bridges between components, allowing them to communicate in a clear and fast way, whether wired (e.g. LIN, SENT) or wireless (RKE, RFID).

Melexis is headquartered in Belgium and employs over 1,100 people in 19 locations worldwide. The company is publicly traded on Euronext Brussels (MELE).

For more information, visit www.melexis.com

On behalf of the entire Organizing Committee, it is our pleasure to welcome you to the 47th European Solid-State Device Research Conference (ESSDERC) and the 43rd European Solid-State Circuits Conference (ESSCIRC) 2017. ESSDERC-ESSCIRC finally returns back to the university town of Leuven, Belgium, many years after having organised a successful ESSDERC-ESSCIRC Conference in 2004 and ESSDERC Conferences in 1999 and 1992, respectively. Since 2003 both ESSDERC and ESSCIRC are running in parallel and have joint keynote speakers and joint focus sessions. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers and system designers. As participant to ESSDERC and ESSCIRC, you not only have the opportunity to become familiar with the latest advances in these fields, but you will meet people who pioneered previous developments, you get access to enhance your international network in micro/nanoelectronics and you will be a witness to previews into emerging fields.

The conference takes place downtown in the city of Leuven, which up to the end of the 13rd century the residence of the Dukes of Brabant. Today Leuven is still the capital of the province of Flemish Brabant. Since 1425 Leuven is the home of KU Leuven, with its ~56000 students the largest university in Belgium. The majority of these students reside in Leuven, and this includes 16% international students. The presence of imec, the largest independent research center in Europe with over 3500 researchers coming from more than 70 different countries, brands Leuven as a world leading hub for micro- and nano-electronics.

This year ESSDERC-ESSCIRC received a total of 393 submissions from 36 countries, of which 241 contributed ESSCIRC and 153 contributed and track invited ESSDERC submissions. About 52% of the submissions came from Europe, 28% from Asia/Pacific and 18% from North America, clearly demonstrating the international character of the conference.

The conference has 4 plenary keynote speakers (Melexis, ON Semiconductor, Analog Devices and Tohoku University), 3 ESSDERC plenary speakers (Intel, SanDisk and RWTH Aachen) and 3 ESSCIRC plenary speakers (Nokia Bell Labs, Ericsson and Columbia University). The selected papers are presented in 43 regular sessions and two focus sessions on Neuromorphic Computing and Quantum Computing, respectively. All this is spread over three days of oral presentations, Tuesday September 12 to Thursday September 14.

The program also includes an extraordinary social program with a welcome reception and a conference banquet, both with surprise acts. These social events will offer ample opportunities for networking.

In addition, the first day of the event on Monday September 11 will be dedicated to 5 tutorials (1 full-day and 2 half-day tutorials organized by ESSDERC and 2 full-day tutorials organized by ESSCIRC) and to 4 workshops, organized by European and international research and industry consortia. These give extra opportunities for update your knowledge of the state of the art in the covered areas.

We thank the IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) that are the official sponsors of ESSCIRC and ESDERC, respectively. We also thank all external sponsors that have provided the extra means allowing us to offer the little extras that beyond doubt will make ESSDERC-ESSCIRC 2017 a memorable event in a long tradition.

We are very grateful to the excellent collaboration with the exceptional members of the Organizing Committee and the Technical Program Committee. All members have extremely been devoted and have worked very hard to make ESSDERC-ESSCIRC 2017 yet another successful event. Without their dedication, enthusiasm and professionalism this would not have been possible. We also thank all collaborators and volunteers that helped us out.

Finally, the real success of a conference is based on the support of all the authors who submitted papers to the conference and on the willingness of the keynote, invited, focus session and tutorial speakers to travel to Leuven and to share their knowledge and insights. Their support and efforts are highly appreciated.

Enjoy the 2017 edition of ESSDERC-ESSCIRC and your visit to Leuven, Belgium, and after enjoying and savoring this year's program, we hope to see you all again in Dresden, Germany, for ESSDERC-ESSCIRC 2018.

Jo De Boeck and **Georges Gielen**
Conference General Chairs – ESSDERC-ESSCIRC 2017

Marc Heyns and **Guido Groeseneken**
TPC Chairs – ESSDERC 2017

Wim Dehaene and **Patrick Reynaert**
TPC Chairs – ESSCIRC 2017

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Track 2: Opto-, Power- and Microwave Devices

- **Mikael Östling** - KTH — Track Chair

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- Edwin Piner - Texas State University
- Gianmauro Pozzovivo - Infineon
- Susanna Reggiani - University of Bologna
- Tetsuya Suemitsu - Tohoku University
- Florian Udrea - Cambridge University

Track 3: Fundamental Physical Modeling of Materials and Devices

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- Herve Jaouen - STMicroelectronics
- Juergen Lorenz - Fraunhofer IISB
- Bernd Meinerzhagen - TU Braunschweig
- Victor Moroz - Synopsis
- Phil Oldiges - IBM
- Massimo Rudan - University of Bologna
- Enrico Sangiorgi - University of Bologna
- Viktor Sverdlov - TU Wien
- Francois Triozon - CEA-LETI

Track 4: Device and Circuit Compact Modeling

- **Wladek Grabinski** - MOS-AK — Track Chair
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- Yogesh Chauhan - IIT Kanpur
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- Ehrenfried Seebacher - AMS
- Daniel Tomaszewski - ITE Warsaw
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- Zhiping Yu - Tsinghua University
- Xing Zhou - NTU

Track 5: Advanced and Emerging Memories

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- Georg Tempel - Infineon
- Elisa Vianello - CEA-LETI
- Dirk Wouters - RWT Aachen

Track 6: MEMS, NEMS, Bio-sensors and Display Technologies

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- Radu Sporea - University of Surrey

Track 7: Emerging non-CMOS Devices and Technologies

- **MaxLemme** - University of Siegen — Track Chair

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- Costin Anghel - ISEP
- Kees de Groot - University of Southampton
- Thomas Ernst - CEA-LETI
- Gianluca Fiori - University of Pisa
- Elena Gnani - University of Bologna
- Steve Hall - University of Livepool
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- Eric Pop - Stanford University
- Heike Riel - IBM Zürich
- Andreas Schenk - ETH Zürich
- Hitoshi Wakabayashi - Tokyo Institute of Technology
- Grace Xing - Cornell University
- Thomas Zimmer - IMS Bordeaux

WELCOME TO LEUVEN

With about 100.000 inhabitants, Leuven is well known as a university city. It is the home of the biggest university in Belgium, with more than 40.000 students. Founded in 1425 by Papal Bull under Martinus V, it is also the oldest university in Belgium.

The city of Leuven itself came in full bloom a few centuries earlier. Up to the end of the 13rd century, it was the residence of the Dukes of Brabant. Town and university have known many periods of prosperity. The town hall, churches, cloisters and colleges stand silent witness of those days and make Leuven an interesting place, rich in historical buildings that radiate a magic of their own. Major tourist attractions are the more than 550 year old town hall, the Great Beguinage, the University Library, the St. Peters Cathedral and the Papal college.

Triggered by the presence of imec, the largest independent research center in Europe with over 3500 researchers coming from more than 70 different countries, Leuven became a world leading center for micro and nano-electronics. KU Leuven and imec have created almost 200 spin-off companies. Leuven is also hosting the headquarters of AB INBEV, the largest brewery in the world.

Leuven is only 20 km away from Brussels, the capital of Belgium and hearth of Europe. It is ideally situated to visit world famous places like Antwerp, Gent and Bruges. Even the seaside or the Ardennes are less than 2 hours away.

The venue of the conference events, including workshops and tutorials, will be in the center of Leuven.

GETTING AROUND LEUVEN

By Bus

The main local bus terminal is located next to the railway station (if you leave the station, it is on your right hand side). The busses easily reach Leuven centre and surrounding areas. Local busses are run by De Lijn (www.delijn.be)

By Bike

You can hire bikes at a number of different locations in Leuven. (www.visitleuven.be/en/bike)

By Taxi

Taxis can be found at the Leuven train station (in front of the main building) and at Smoldersplein (near the courthouse).

Taxi companies in Leuven:

- Taxi Alex
  Bierbeekstraat 116, 3001 Leuven (Heverlee),
  Tel. +32 16 29 16 16
- Taxi's Jenny NV
  Diestsesteenweg 489, 3010 Leuven (Kessel-Lo),
  Tel. +32 16 25 35 65
- Taxi Gerard
  Wipstraat 27, 3010 Leuven (Kessel-Lo),
  Tel. +32 16 25 09 99
- Cordons-Van Minsel BVBA
  Hoveniersdreef 31, 3001 Leuven (Heverlee),
  Tel. +32 16 22 20 00

KU LEUVEN CAMPUS OF SOCIAL SCIENCES

The ESSCIRC/ESSDERC Conference takes place in the city center of Leuven, at the:

KU LEUVEN Campus of Social Sciences
Parkstraat 45, 3000 Leuven, Belgium

HOW TO REACH THE VENUE

From the train station

By Foot

The Faculty of social Sciences is situated at walking distance (about 15 minutes) from the station. Follow 'Maria-theresiastraat' until it changes into 'Andreas Vesaliusstraat'. Then follow the 'Andreas Vesaliusstraat' up to the crossing with the 'Parkstraat'. Turn right here.
You will find the campus about 100m further at your right side.

By bus

Take the bus with number 4, 5 or 6 and alight at the stop called 'Remy' in the 'Andreas Vesaliusstraat'. Follow the 'Andreas Vesaliusstraat' until it crosses with the 'Parkstraat'. Then turn right. You will find the campus about 100m further at your right side.

SESSIONS

Sessions will be located in different buildings inside and just outside the Campus:

- **JOINT PLENARY SESSIONS**
  VESALIUS AULA (Andreas Vesaliusstraat, 3000 Leuven), just outside the Campus. The Andreas-Vesalius street is the continuation of the Maria-Theresiastreet and connects the campus directly to the train station.

- **ESSCIRC SESSIONS**
  Room **AP 00.15** Auditorium Max Weber (**AP**)
  (Parkstraat 51, 3000 Leuven) inside the Campus
  Room **AV 91.12** Auditoria complex (**AV**)
  (Parkstraat 49, 3000 Leuven) inside the Campus
  Room **AV 01.12** Auditoria complex (**AV**)
  (Parkstraat 49, 3000 Leuven) inside the Campus
  Room **AV 03.12** Auditoria complex (**AV**)
  (Parkstraat 49, 3000 Leuven) inside the Campus

- **ESSDERC SESSIONS**
  Room **AP 01.30** Auditorium Jean Monnet (**AP**)
  (Parkstraat 51, 3000 Leuven), same building as Max Weber Auditorium but upstairs, inside the Campus
  Room **AV 00.17** Auditoria complex (**AV**)
  (Parkstraat 49, 3000 Leuven) inside the Campus
  Room **AV 02.17** Auditoria complex (**AV**)
  (Parkstraat 49, 3000 Leuven) inside the Campus

- **TUTORIALS** (Monday 11 September)
  Room **AV 01.12** Integrated Power Management in Research and Industry
  Room **AV 03.12** The Hidden Challenges of 5g
  Room **AV 00.17** Beyond Cmos
  Room **AV 02.17** Sensors for the Iot Era
  Room **AV 02.17** Neuromorphic Computing with Emerging Synaptic Devices

- **WORKSHOPS** (Monday 11 September)
  Room **AV 04.17** Connect
  Room **AV 91.12** Mos-AK
  Room **AP 00.15** Sinano - Nereid
  Room **AP 01.30** Semiconductor Memories

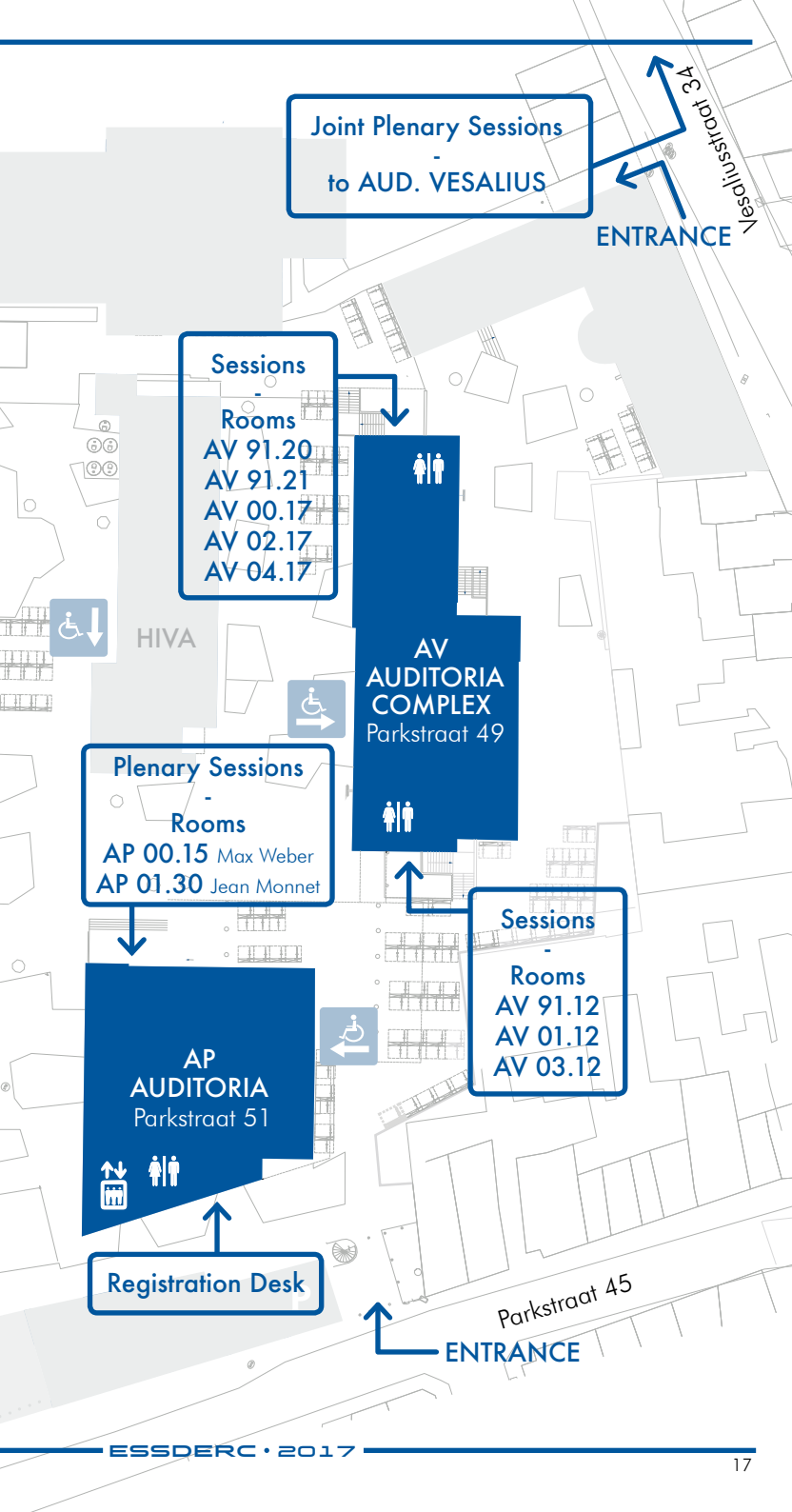
- **WOMEN IN CIRCUITS** (Tuesday at 12:30 pm)
  At FlexiSpace inside KU Leuven Agorà Learning Centre (E. Van Evenstraat 4 - B-3000 Leuven) in the KU LEUVEN Campus of Social Sciences

- **ELECTRONIAD QUIZ** (Tuesday at 7:00 pm)
  Alma 2 - E. Van Evenstraat 2, Leuven

- **REGISTRATION DESK**
  The Registration Desk will be located in the Max Weber/ Jean Monnet building (AP Auditoria).
  Registration Desk will move to VESALIUS AULA only on Tuesday from 8.00 till 10.00 am.

- **COFFEE BREAKS AND LUNCHES**
  Breaks will be held in the Student Restaurant Alma 2 (Parkstraat 45, inside the Campus), which will be closed for the public during the conference.


AGORA LEARNING CENTRE
E. Van Evenstraat
FACULTY OF SOCIAL SCIENCES
ALMA 2
Lunch
&
Coffee
REHS


Joint Plenary Sessions
-
to AUD. VESALIUS
ENTRANCE
Vesaliusstraat 34
Sessions
-
Rooms
AV 91.20
AV 91.21
AV 00.17
AV 02.17
AV 04.17
HIVA
AV
AUDITORIA
COMPLEX
Parkstraat 49
Plenary Sessions
-
Rooms
AP 00.15 Max Weber
AP 01.30 Jean Monnet
Sessions
-
Rooms
AV 91.12
AV 01.12
AV 03.12
AP
AUDITORIA
Parkstraat 51
Registration Desk
Parkstraat 45
ENTRANCE

Morning Tutorials - Monday September 11th, 2017

Time	AV01.12	AV03.12	AV00.17	AV02.17
	ESSCIRC Tutorials		ESSDERC Tutorials	
	Integrated Power Management in Research and Industry	The Hidden Challenges of 5G	Beyond CMOS	Sensors for the IoT Era
08:00-08:30	Registrations	Registrations	Registrations	Registrations
08:30-09:00				Introduction and Overview *Mirjana Banjevic*
09:00-10:00	Integrated Switched-capacitor Power Converters: a Feasible Way to Get High Efficiency Power Conversion in Standard CMOS Technology *Gerard Villar Piqué*	What is Required of 5G to Make It Attractive for MTC? *Yao-Hong Liu*	Introduction to Beyond CMOS *Iuliana P. Radu*	Smart Sensors for Environmental Monitoring *Florin Udrea*
10:00-10:30	Coffee Break			
10:30-11:30	Integrated Inductive and Hybrid DC-DC Converters *Giovanni Frattini*	Programmable mm-Wave Transmitters: Generalized PA Architectures for Frequency and Back-off Reconfigurability *Kaushik Sengupta*	Tunnel FETs – Status and Prospects *Nadine Collaert*	Sensors for Health Monitoring *Patrick Mercier*
11:30-12:30	Making Magnetics Disappear - Integrated Magnetics for Power Management *Cian O'Mathuna*	Implementing Massive MIMO Systems: Coarse Processing Gives Fine Performance *Liesbet Van der Perre*	Negative Capacitance FETs: Physics, Materials and Devices *Asif Islam Khan*	Sensors for Automotive Industry *Appo van der Wiel*
12:30-13:30	Lunch			

Afternoon Tutorials - Monday September 11th, 2017				
Time	AV01.12	AV03.12	AV00.17	AV02.17
	ESSCIRC Tutorials		ESSDERC Tutorials	
	Integrated Power Management in Research and Industry	The Hidden Challenges of 5G	Beyond CMOS	Neuromorphic Computing with Emerging Synaptic Devices
12:30-13:30	Lunch			Lunch
13:30-14:00				Neuro-inspired Computing using Resistive Synaptic Devices: Challenges and Prospects *Shimeng Yu*
14:00-15:00	Vibrational Harvesters for Wireless Sensing Applications *Stefano Stanzione*	Integrated Wide-band Baseband Filters and Narrow-band RF Filters for 5G *Bram Nauta*	Towards Functionality-Enhanced Devices: Controlling the Modes of Operations in Three-Independent-Gate Transistors *Pierre-Emmanuel Gaillardon*	Analog Synapse Devices based on Interface Resistive Switching for Neuromorphic Systems *Hyunsang Hwang*
15:00-15:30	Coffee Break			
15:30-16:30	Power Management Design for Highly Integrated Automotive ICs *Bernhard Wicht*	Challenges in 5G Transmitter Design *Christian Fager*	Spintronics in the Context of Computation *Titash Rakshit*	Emerging Memories for Neurocomputing *Dmitri Strukov*
16:30-17:30	1 kV On-chip, Hard to Resist? *Valentijn De Smedt*	Opto Implementation Challenges for 5G Networks *Francesco Testa*	Introduction to Quantum Computing *Ronald Hanson*	Accelerating Backpropagation Training with Non-Volatile Memory: Devices, Circuits and Architecture *Geoffrey Burr*

Workshops - Monday September 11, 2017

AV 04.17	AV 91.12	AP 00.15	AP 01.30
08:00 Registrations	08:00 Registrations	08:00 Registrations	
08:30 - 10:10 CONNECT *Aida Todri-Sanial* *Salvatore M. Amoroso* *Benjamin Uhlig* *Gage Krieger Hills* *Esko Kauppinen*	08:30 - 10:10 MOS-AK *Jim Greer* *Marcelo Pavanello*	09:00 - 10:45 SINANO - NEREID *Enrico Sangiorgi* *Francis Balestra* *Francisco Ibanez* *Jouni Ahopelto* *Clivia Sotomayor Torres*	08:30 - 11:15 SEMICONDUCTOR MEMORIES *Francisco Gamiz* *Kilho Lee* *Manfrest Horstman* *Elisa Vianello*
Coffee 10:10 - 10:40	Coffee 10:10 - 10:30	Coffee 10:45 - 11:00	Coffee 11:15 - 11:45
10:40 - 12:30 CONNECT (Continued) *Jean Dijon* *Benjamin Uhlig* *Marleen van der Veen*	10:30 - 12:30 MOS-AK *Wim Schoenmaker* *Jean-Pierre Raskin* *Chika Tanaka*	11:00 - 12:45 SINANO - NEREID (Continued) *Anda Mocuta* *Yann Deval* *Montserrat Fernandez-Bolanos* *Steve Stoffels* *Stéphane Monfray*	11:45 - 13:15 SEMICONDUCTOR MEMORIES (Continued) *Pierre Fazan* *Guohan Hu*
Lunch 12:30 - 14:00	Lunch 12:30 - 14:00	Lunch 12:45 - 14:00	Lunch 13:15 - 14:30
14:00 - 15:10 CONNECT (Continued) *Shu-Jen Han* *Bingan Chen*	14:00 - 15:00 MOS-AK (Continued) *Nicolas Cordero* *Ashkhen Yesayan*	14:00 - 16:00 SINANO - NEREID (Continued) *Danilo Demarchi* *Holger Schmid* *Georgios Fagas* *Thanasis Dimoulas* *Enrico Sangiorgi*	14:30 - 16:00 SEMICONDUCTOR MEMORIES (Continued) *Philippe Galy* *Sorin Cristoloveanu* *Joris Lacord*
Coffee 15:10 - 15:40	Coffee 15:00 - 15:30		Coffee 16:00 - 16:30
15:40 - 17:00 CONNECT (Continued) *Bernd Gotsmann* *Aida Todri-Sanial*	15:30 - 17:00 MOS-AK (Continued) *Denis Flandre* *Benjamin Iniguez* *Saravana Maruthamuthu*		16:30 - 17: 45 SEMICONDUCTOR MEMORIES (Continued) *Asen Asenov* *Andy Pickering*

Tuesday September 12th, 2017

Time	AP00.15	AV91.12	AV01.12	AV03.12	AP01.30	AV00.17	AV02.17
08:00-08:30	Vesalius -- Registrations						
08:30-09:00	Vesalius -- Conference Opening & Welcome (presentation by SSC society and EDS society)						
09:00-09:40	Vesalius -- A1L-A: ESSDERC/ESSCIRC Joint Plenary 1: Françoise Chombar, Melexis Engineering a Safe, Clean & Comfortable Future						
09:40-10:20	Vesalius -- A2L-A: ESSDERC/ESSCIRC Joint Plenary 2: Peter Real, Analog Devices Navigating without a Moore's Law Compass						
10:20-11:00	Coffee Break						
11:00-12:20	A3L-B References	A3L-C RF Receivers and Detectors	A3L-D Digital Accelerators	A3L-E Optical Sensors	A3L-F Resistive RAM	A3L-G Cross-Domain Compact Modelling	A3L-H Focus Session: Beyond CMOS Devices I
12:20-14:00	Lunch						
14:00-15:20	A4L-B Amplifiers and Comparators	A4L-C Oscillators	A4L-D Wireline and Optical		A4L-F Alternative Device Simulations	A4L-G Parameter Extraction	A4L-H Focus Session: Beyond CMOS Devices II
15:20-15:50	Coffee Break						
15:50-16:30	Room: AP00.15 A5L-B, ESSCIRC Keynote 1: Yves Baeyens: Solving Capacity Bottlenecks in Fixed Access Comms				Room: AP01.30 A5L-F, ESSDERC Keynote 1: Ian Young: Principles and Trends in Quantum Nano-Electronics & Nano-Magnetics for Beyond-CMOS Computing		
16:40-18:00	A6L-B Energy Harvesting	A6L-C Advanced ADC Techniques	A6L-D Digital-intensive Frequency Synthesis	A6L-E Digital Processors		A6L-G Modelling of Emerging Devices	A6L-H 2D Material Devices
18:00-19:00	ESSCIRC TPC Mtg.				ESSDERC TPC Mtg.		
19:00-21:00	ESSDERC/ESSCIRC 2017 Welcome Reception: Jubilee Hall						

Legend CIRC = CIRC Keynote = DERC = DERC Keynote = Joint =

Wednesday September 13th, 2017

Time	AP00.15	AV91.12	AV01.12	AV03.12	AP01.30	AV00.17	AV02.17
08:30-08:45	Vesalius -- Presentation on ESSCIRC/ESSDERC 2018						
08:45-09:25	Vesalius -- B1L-A: ESSDERC/ESSCIRC Joint Plenary 3: Hans Stork, ON Semiconductor Smart Power for Automotives						
09:25-10:10	Coffee Break						
10:10-12:10	B2L-B High Speed ADC	B2L-C Transmitters and Power Amplifiers for mm-Wave and IoT	B2L-D Biomedical Circuits and Systems		B2L-F Widebandgap Power Devices	B2L-G Advanced CMOS Characterization and Reliability	B2L-H Emerging Memory Technologies
12:10-13:30	Lunch						
13:30-14:10	Room AP00.15 B3L-B, ESSCIRC Keynote 2: Sven Mattisson, Ericsson - Overview of 5G Requirements & Future Wireless Networks				Room AP01.30 B3L-F, ESSDERC Keynote 2: Siva Sivaram - Storage Class Memories: Desire Meets Reality		
14:20-15:40	B4L-B High Efficiency ADC	B4L-C 5G and mm-Wave Frequency Synthesis	B4L-D Machine Learning and Neuromorphic Computing	B4L-E Linear Regulators	B4L-F FinFEt and Nanowire Simulations	B4L-G Traps and Noise	B4L-H 2D Material Integration
15:40-16:00	Coffee Break						
18:00-23:00	Gala Dinner: Autoworld (Brussels)						

Legend CIRC = CIRC Keynote = DERC = DERC Keynote = Joint =

Thursday September 14th, 2017

Time	AP00.15	AV91.12	AV01.12	AV03.12	AP01.30	AV00.17	AV02.17
08:30-09:00	Vesalius -- Awards Ceremony						
09:00-09:40	Vesalius -- C1L-A: Joint Plenary 4: Tetsuo Endoh, Tohoku University Spintronics Applications: STT-MRAM & Non Volatile Logic						
09:40-10:20	Coffee Break						
10:20-12:00	C2L-B Power Management and Harvesting	C2L-C Embedded Memories	C2L-D Wireless SOC	C2L-E Focus Session: Neuromorphic Computing	C2L-F Photonics / Microwave / Harsh Enviroment	C2L-G Advanced CMOS Technology	C2L-H Microfluidics and TFTs
12:00-13:30	Lunch						
13:30-14:10	Room AP00.15 C3L-B, ESSCIRC Keynote 3: Harish Krishnaswamy, Columbia Univ. - Integrated Antenna-Interface Components				Room AP01.30 C3L-F, ESSDERC Keynote 3: David DiVincenzo - Control Systems for Quantum Computers		
14:20-15:40	C4L-B DC-DC Converters	C4L-C Sensor Interfaces	C4L-D Low Power Radios		C4L-F Modelling and Measurement of Alternative Material Devices	C4L-G High Mobility Materials and Nanowires	C4L-H Focus Session: Quantum Computing
19:00	ELECTRONIAD Quiz – Celebrating Easics 25th Anniversary						

Legend: CIRC = | CIRC Keynote = | DERC = | DERC Keynote = | Joint =

LANGUAGE

The official language of the conference is English: no simultaneous translation will be available.

REGISTRATION DESK

The Registration Desk will be located in the Max Weber/Jean Monnet building (AP Auditoria) and it will be open the following hours throughout the Conference:

- Monday 11 September: 8.00 am - 6.00 pm
- Tuesday 12 September: 8.00 am - 5.00 pm
- Wednesday 13 September: 8.00 am - 4.00 pm
- Thursday September: 9.00 am - 4.00 pm

Registration Desk will move to VESALIUS AULA only on Tuesday from 8.00 till 10.00 am.

BADGES

Badges must always be visibly worn during sessions, coffee breaks and lunches, and also during social program activities.

COFFEE BREAKS AND LUNCHES

Coffee breaks and lunches will be served to registered participants wearing their badges. Accompanying persons have no access to scientific sessions nor to coffee breaks and lunches. Please note that vegetarian dishes will be on daily menu; for other special needs, we will try to serve a good variety of food so that it will be easier for you to get some alternatives in case of special diet restrictions.

PERSONS WITH SPECIAL NEEDS

Every effort has been made to ensure that people with special needs are catered for during the conference. Should you require any specific assistance, please let us know in advance to enable to assist in making your stay at the conference a pleasant and comfortable one.

INTERNET / WI-FI

Wi-Fi connection will be available on site.

CERTIFICATE OF ATTENDANCE

Certificates will be sent by email upon request to essxxrc@sistemacongressi.com, after the Conference.

LIABILITY
In registering for the conference, participants agree that neither the Scientific/Organizing Committees nor the Organizing Secretariat assumes any liability.

CURRENCY
The local currency is € (Euro). Automatic teller machines and exchange offices are available in Leuven city centre. Most hotels, restaurants and shops accept major credit cards but please always check first!

ELECTRICITY
Electricity is 220-230V, 50 Hz. Belgian plugs have two round pins.

CALLING CODES
Belgium country code : +32 (or 00 32)
Leuven: +32 (0)16

EMERGENCY NUMBERS
European emergency number: 112

PHARMACY APOPARK
Address: Tiensestraat 81, 3000 Leuven
Phone: 016/22.20.48 Website
Opening hours: Mo - Fr: 8.30 am - 18.00 pm, Sa 8.30 am to noon.

STORE OPENING HOURS
Most shops are open from Monday till Saturday, 10:00 am - 18:00 pm

SMOKING
No smoking in public places (e.g. airports, train stations, schools, universities, restaurants, bars and cafes, government buildings) and on public transport.

WELCOME COCKTAIL AT JUBILEE HALL

Tuesday 12 September
From 7 pm until 9 pm

It is located in the University Hall, the university's main building in the city centre.

University Hall, Naamsestraat 22, Leuven

This prestigious building of 1317 was originally the municipal Cloth Hall and only comprised a ground floor in Gothic style. In 1432 the newly founded university was housed in the wing on the Krakenstraat. The hall was used as a lecture hall until the First World War. In 1679 the city sold the entire building to the University that immediately built the baroque first floor. In 1723 the Rega wing was added (classical sandstone façade overlooking Oude Markt).

Rate
Free for conference participant
Additional Welcome Cocktail ticket: € 30,00

GALA DINNER AT AUTOWORLD

Wednesday 13 September
From 6 pm until 11.30 pm

Jubelpark 11, 1000 Brussels

The museum's housing treasures of the history of the motor car, thanks to Ghislain Mahy's and his family's gamble, and the gentle but uncontested force of persuasion of a prince who later became King Albert II. They were helped by the combined support of the ministerial responsibilities of the late vice-president of Autoworld, Minister Louis Olivier, formerly in charge of public works, and President Herman De Croo, communications minister for eight years. Autoworld is a highly-colorful environment adapted for teaching purposes and created to continue evolving on a non-stop basis.
Decades of evolution in technology, comfort, safety and increasing concern with the environment are on display here via superb coaches and countless motorized vehicles. From the earliest models of the distant past to contemporary cars that prefigure the automobile of tomorrow and beyond, the visitor is guided through the fabulous history of the motor car thanks to technical but easily comprehensible commentaries.

Rate

Free for conference participant
Additional Gala Dinner ticket: € 150,00

How to get

Buses will be provided from Leuven to Autoworld and back (no intermediate stops will be possible). Information will be available at the registration desk.

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

ESSDERC 2017 Tracks

- Advanced CMOS: Process and Device Technology, Characterization and Reliability
- Opto-, Power and Microwave Devices.
- Fundamental Physical Modeling of Materials and Devices
- Device and Circuit Compact Modeling
- Advanced and Emerging Memories
- MEMS, NEMS, Bio-sensors and Display Technologies
- Emerging non-CMOS Devices and Technologies

ESSDERC/ESSCIRC Focus Tracks

- Neuromorphic Computing
- Quantum Computing

FRANÇOISE CHOMBAR

CEO Melexis, Belgium

Engineering a safe, clean and comfortable future

Ms. Françoise Chombar has been the Chief Executive Officer of Melexis NV, since 2004 and has been its Managing Director since February 15, 2011. Ms. Chombar serves as the Chief Executive Officer of Melexis Microelectronic Integrated Systems N.V. She is the Co-Founder of Melexis. Ms. Chombar served as Chief Operating Officer of Melexis NV since 1994. She served as Chief Executive Officer for Operations, Sales and Human Resources of Epiq Nv since 2004 and its Acting Chief Operating Officer since 1994. She served as Planning Manager at Elmos GmbH, a German semiconductor company, from 1986 to 1989 and as Commercial Assistant at Michel Vande Wiele n.v., a Belgian textile equipment manufacturer, from 1984 to 1985. Since 1989 she served as a Operations Manager of Elex-Xtrion group since 1989. Ms. Chombar has been a Director of Epiq NV since 1996 and Melexis NV since 1996. She has been an Independent Non-Executive Director of Umicore S.A. since April 26, 2016. She served as an Independent Director of EVS Broadcast Equipment S.A. since May 2012. She served as a Director of Elex-Xtrion group. She's been mentor of the Women's network Sofia since 2000, a member of Women on Board since 2011 and honorary ambassador of the Department of Applied Languages of the University of Gent since January 2012.

Ms. Chombar holds a Master Degree as Interpreter in Dutch, English and Spanish from the University of Gent.

TETSUO ENDOH
Professor Tohoku University, Japan

Spintronics applications: STT-MRAM and Non Volatile Logic

Tetsuo Endoh joined ULSI Research Center Toshiba Co. in 1987 and was engaged in the R&D of NAND Memory. He became a lecturer at the Research Institute of Electrical Communication, Tohoku University in 1995. He is a professor at the Department of Electrical Engineering, the Graduate School of Engineering, Tohoku University and director of the Center for Innovative Integrated Electronic Systems (CIES). His current interests are novel 3D structured device technology, such as Vertical MOSFETs; high-density memory, such as SRAM, DRAM, 3D-NAND memory and STT-MRAM; and beyond-CMOS technology, such as spintronics-based non-volatile Logic for ultralow power systems such as mobile systems, AI systems and IoT systems.

He is also interested in power-management technology, such as GaN on Si based power devices and power integrated circuits with low energy loss and low power consumption for automotive applications. He received the 14th Prime Minister's Award for its Contribution to Industry-Academia-Government Collaboration in 2016. He received 2017 National Invention Award "the 21st century Encouragement of Invention Prize" on June 12th.

PETER REAL

Senior VP & CTO Analog Devices Inc.

Navigating without a Moore's Law Compass

Peter Real is Senior Vice President and Chief Technology Officer of Analog Devices. In this role, Mr. Real works closely with ADI's business units and manufacturing operations to provide a long term technology and capability vision for the company which drives ADI's competitive advantage. He is responsible for the identification, sourcing, and nurturing of new business, technology, and research opportunities while also being responsible for the development of foundation capabilities in support of current and future needs. Previously, Mr. Real held the positions of Vice President of the High Speed Products and Technology Group, Vice President of the Linear and Radio Frequency Products and Technology Group, Vice President of the Radio Frequency and Networking Products Group, and various design engineering and product line leadership roles.

Mr. Real holds Bachelor of Science and Master of Science degrees in Electrical Engineering, and is the author or co-author of nine patents.

HANS STORK

Senior VP & CTO ON Semiconductor, USA

Smart Power for Automotives

Dr. Hans Stork is Senior Vice President and Chief Technology Officer (CTO) at ON Semiconductor. He oversees the development of wafer process technologies, modeling and design kits, design libraries, as well as packaging technologies and assembly support.

Prior to joining ON Semiconductor, Dr. Stork was Group Vice President and CTO of the Silicon Systems Group at Applied Materials. From 2001 to 2007 he was Senior Vice President and the CTO of Texas Instruments. Before that, Dr. Stork held various R&D and management positions at Hewlett Packard Laboratories and at IBM's T.J. Watson Research Center.

Dr. Stork serves on the supervisory board of ASML, is a member of the Scientific Advisory board at imec, and has previously served on the boards of Sematech and the SRC. He is also a longstanding member of the SIA Technology Strategy Committee. He authored more than 100 cited papers and holds 11 U.S. patents. He was elected IEEE Fellow in 1994, and served on several IEEE sponsored conference program committees, and is currently vice-chair of the Technical Field Awards Council and a member of the Awards Policy and Portfolio Review Committee.

Dr. Stork was born in Soest, The Netherlands, and received the Ingenieur degree in electrical engineering (EE) from Delft University of Technology, Delft, The Netherlands, and holds a PhD in EE from Stanford University.

DAVID DIVINCENZO

Professor RWTH, Aachen, Germany

Control Systems for Quantum Computing

David DiVincenzo was one of the first physical scientists to engage in quantum information research.

His name is associated with the development of criteria for the physical implementation of a quantum computer, known as the DiVincenzo Criteria. As part of the Jülich Aachen Research Alliance (JARA), DiVincenzo is the head of the Institute of Quantum Information at RWTH Aachen University; he is also head of the Institute of Nanoelectronics at the Forschungszentrum Jülich. His PhD was in Electrical Engineering at the University of Pennsylvania; after a postdoc at Cornell, he was a Research Staff Member and Research Manager at IBM TJ Watson Research Center, Yorktown Heights, New York, for 25 years.

He is a Fellow of the American Physical Society, Associate Editor of the Reviews of Modern Physics, and von Humboldt Professor.

SIVA SIVARAM
SanDisk Corp., Executive VP, USA

Storage Class Memories: Desire Meets Reality

Dr. Siva Sivaram was appointed executive vice president of memory technology in May 2016 when SanDisk was acquired by Western Digital and is responsible for the ongoing development of the company's industry-leading NAND flash memory, as well as the development of next-generation technologies, including 3D NAND (BiCS) and 3D ReRAM. Sivaram has over 30 years of experience in semiconductors, 3-D memory architectures, process technology, equipment and materials. He has held executive positions at Intel and Matrix Semiconductor, and at SanDisk after its acquisition of Matrix. Additionally, he was the Founder and CEO of Twin Creeks Technologies, a solar panel and equipment company.

Under his leadership, SanDisk created the world's first cross point 3D memory technology, the world leading 15nm 2D NAND technology, and the industry's first 256 Gigabit (Gb) 3-bit-per-cell (X3) 48-layer 3D NAND chip.

Sivaram has also served as a board member of several start-up firms, was entrepreneur-in-residence at Crosslink Capital and XSeed Capital, a research scholar at Matsushita Electric, and an adjunct faculty member at San Jose State University.

Additionally, Sivaram has published numerous technical papers as well as a textbook on Chemical Vapor Deposition, and he holds several patents. He earned his doctorate and master's degrees in materials science from the Rensselaer Polytechnic Institute where he has been elected to its Board of Trustees. He is a Distinguished Alumnus of the National Institute of Technology, Tiruchi, India, where he earned his bachelor's degree in mechanical engineering.

IAN YOUNG
Intel, Senior Fellow, USA

Principles and Trends in Quantum Nano-Electronics and Nano-Magnetics for Beyond-CMOS Computing

Ian Young is a Senior Fellow and director of Exploratory Integrated Circuits in the Technology and Manufacturing Group of Intel Corporation. He joined Intel in 1983 and his technical contributions have been in the design of DRAMs, SRAMs, microprocessor circuit design, Phase Locked Loops and microprocessor clocking, mixed-signal circuits for microprocessor high speed I/O links, RF CMOS circuits for wireless transceivers, and research for chip to chip optical I/O. He has also contributed to the definition and development of Intel's process technologies.

He now leads a research group exploring the future options for the integrated circuit in the beyond CMOS era. His recent work developed a uniform benchmarking methodology to identify the key technology options in quantum nano-electronics and nano-magnetics such as tunneling junction field-effect devices and spintronics.

Ian Young received the Bachelor of Electrical Engineering and the Master Eng. Science, from the University of Melbourne, Australia. He received the PhD in Electrical Engineering from the University of California, Berkeley. He is the recipient of the 2009 International Solid-State Circuits Conference's Jack Raper Award for Outstanding Technology Directions paper. He is a Fellow of the IEEE.

- **COLIN MCANDREW**
  NXP Semiconductors, Phoenix, AZ, USA

  SPICE Modeling in Verilog-a: Successes and Challenges

- **BENOÎT SKLÉNARD**
  CEA Leti, MINATEC Campus, Grenoble, France

  Advances in the Understanding of Microscopic Switching Mechanisms in ReRAM Devices

- **TANYA NIGAM**
  GLOBALFOUNDRIES, Santa Clara, CA, USA

  Material and Device Innovation Impact on Reliability for Scaled CMOS Technologies

- **GIORGIO SERVALLI**
  Micron Technology, Vimercate, Italy

  Emerging Memory Technologies for High Density Applications

- **FRANCESCO BONACCORSO**
  Istituto Italiano di Tecnologia, Genova, Italy

  Ink-jet Printed 2D Crystal Heterostructures

- **VEERESH DESHPANDE**
  IBM Research Zurich, Switzerland Hybrid InGaAs/SiGe

  CMOS Circuits with 2D and 3D Monolithic Integration

- **SÉVERINE LE GAC**
  University of Twente, Enschede, The Netherlands

  Microfluidic Technology: New Opportunities to Develop Physiologically Relevant in vitro Models

- **GUANGRUI XIA**
  University of British Columbia, Vancouver, Canada

  Dopant Diffusion and Segregation, Si-Ge Interdiffusion and Defect Engineering in SiGe Devices

All tutorials will be held on Monday 11 September.
08.00 - 09.00 Registrations

- BEYOND CMOS -

Tutorial Organizer: Iuliana P. Radu, imec
Room **AV 00.17**

IULIANA P. RADU

09.00 - 10.00

Introduction to Beyond CMOS

Abstract

As we process more and more data which comes from our drive to be always connected, the quest to lower energy usage per computation device is heating up. Si transistor devices have paved the way for the current ubiquity of computation and communication devices but their continued scaling is slowing down. Continues reduction of energy used for computation can come from changing the materials used for transistors, from changing the device concepts, from changing the way we make circuits with novel devices or form completely changing the paradigm of computation. In this tutorial we will review two decide concepts which are expected to work at lower voltage that the classical transistors, the tunnel FET and the negative capacitance FET. We will discuss how increasing the number of gates on a transistor can increase functionality by changing the way circuits are synthesized with these devices. We will review how using not only the charge but also the spin degree of freedom and we will introduce the concept of quantum computing which promises to revolutionize computation through massive intrinsic parallelization.

Bio

Iuliana Radu is Distinguished Member of Technical Staff at imec responsible for Beyond CMOS and Quantum Computing activities at imec. Beyond CMOS activities include work on novel device concepts including spintronics and wave computing and novel materials and their possible applications in the semiconductor industry. Quantum Computing activities includes work on qubit devices and the periphery circuits meant to control them. Prior to establishing the Beyond CMOS programme at imec in 2013, she was a Marie Curie and FWO fellow at KU Leuven and imec. Her work at imec and KU Leuven included devices using the metal to insulator transition, ionic and electronic transport in functional oxides, and devices with graphene and other 2D materials.
Iuliana has received a PhD in Physics from MIT in 2009 where she worked on the Fractional Quantum Hall effect and searched for Majorana fermions. She has received a MSc and a BSc in Physics from University of Bucharest. She has been an author on over 70 papers in leading peer-reviewed journals and conferences. She has given more than 20 invited talks at international conferences and seminars. She is currently a Program Committee member for SISC and SNW.

COFFEE BREAK
10.00 - 10.30

NADINE COLLAERT
10.30 - 11.30

Tunnel FETs – Status and Prospects

Abstract

Over the last decade many reports have looked into tunnel FETs as the ultimate low voltage, low power switch. These devices have in theory the potential to reduce the subthreshold swing below 60mV/dec and as such reduce the operating voltage significantly. While there is still a discrepancy between the theoretical predictions and the performance of the devices, over the last years much progress has been made in the fundamental understanding of the limitations and advantages of these devices, and recent III-V implementations show very promising results. This tutorial will address the advantages and challenges of tunnel FETs, not only focusing on the material and integration aspects but also reviewing the impact of these devices at the circuit level.

Bio

Nadine Collaert received the M.S. and Ph.D. degrees in electrical engineering from the ESAT Department, KU Leuven, Belgium, in 1995 and 2000, respectively. Since then, she has been involved in the theory, design, and technology of FinFET devices, emerging memory devices, transducers for biomedical applications and the integration and characterization of biocompatible materials e.g. carbon-based materials. From 2012 until April 2016 she was program manager of the imec LOGIC program, focusing on high mobility channels, TFET and nanowires. Since April 2016 she is a distinguished member of technical staff, responsible for the research on novel CMOS scaling approaches based on heterogeneous integration of new materials with Si and new material-enabled device and system approaches to increase functionality. She has authored or co-authored more than 300 papers in international journals and conference proceedings, and she holds more than 10 patents in the field of device design and process technology. She has been a member of the CDT committee of the IEDM conference and she is still a member of the Program Committees of the international conferences ESSDERC, ULIS/EUROSOI and VLSI Technology Symposium.

ASIF ISLAM KHAN
11.30 - 12.30

Negative Capacitance FETs: Physics, Materials and Devices

Abstract
Negative capacitance FET (NCFET) is a novel nano-device technology that promises an enormous reduction in power dissipation in post-CMOS electronics. This feat is achieved by replacing the gate dielectric of a MOSFET by a negative capacitance material, which leads to two important effects in the transistor characteristics: sub-60 mV/decade switching and a high on-current. This tutorial will give an overview of the exciting developments in the field of negative capacitance over the past nine years starting from the theoretical prediction in 2008 to the clean experimental demonstration of this phenomenon in ferroelectric materials and transistors recently. All three aspects of this technology: physics, materials and devices will be discussed.

Bio
Asif Khan received his Ph.D. in electrical engineering and computer sciences from the University of California, Berkeley in 2015 and his B.S. degree in electrical and electronic engineering from Bangladesh University of Engineering and Technology (BUET) in 2007. He joined the School of Electrical and Computer Engineering at the Georgia Institute of Technology as a tenure-track assistant professor in the Spring of 2017. Dr. Khan's interests lie at the intersection of electrical engineering, materials science, and the physics of computation. Computing nanodevices that leverage new physics and phenomena in emerging material systems (such as ferro-/anti-ferroelectrics, multiferroics, complex and transition metal oxides and correlated electron systems) are the mainstay of his group. The end goal of his research is to synergize these device-level innovations with existing or new circuits, architectures, and systems concepts such that classical limitations of CMOS platforms can be transcended and new computing paradigms can be envisioned. His work led to the first experimental proof-of-concept demonstration of the negative capacitance–a novel physical phenomenon that can lead to ultra-low power computing and memory platforms by overcoming the fundamental "Boltzmann Limit" of 60 mV/decade subthreshold swing in field-effect transistors.
Dr. Khan received the Qualcomm Innovation Fellowship in 2012, the Silver prize at the 5th Taiwan Semiconductor Manufacturing Company (TSMC) Outstanding Student Research Award in 2011, the University Gold medal from BUET in 2011, Kintarul Haque Gold Medal from BUET in 2011, the 1st prize in IEEE Region 10 Undergraduate Student Paper Contest in 2006, and the 2nd prize in the IEEE History Society Undergraduate Student Paper Contest in 2004.

LUNCH
12.30 - 14.00

PIERRE-EMMANUEL GAILLARDON
14.00 - 15.00

Towards Functionality-Enhanced Devices: Controlling the Modes of Operations in Three-Independent-Gate Transistors

Abstract

Exploiting unconventional physical properties, several nanodevices showed an alternative to Moore's Law by the increase of their functionality rather than the pure scaling. In this tutorial, we will introduce Three-Independent-Gate Field Effect Transistors (TIGFETs), that can, depending on the bias applied to its gate, achieve different modes of operations. The demonstrated modes of operations are (i) the dynamic reconfiguration of the device polarity; (ii) the dynamic control of the threshold voltage; and (iii) the dynamic control of the subthreshold slope beyond the thermal limit (with a measured steep slope of 6mV/dec over 5 decades of current). Such properties are highly desirable for logic computation, as they allow the realization of compact logic gates and circuits beyond the capabilities of CMOS.

Bio

Pierre-Emmanuel Gaillardon is assistant professor in the Electrical and Computer Engineering (ECE) department at The University of Utah, Salt Lake City, UT and he leads the Laboratory for NanoIntegrated Systems (LNIS). Prior to joining the University of Utah, he was a research associate at the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland. He holds a PhD from CEALETI, Grenoble, France and the University of Lyon, France. Prof. Gaillardon is an Associate Editor of the IEEE Transactions on Nanotechnology and is a senior member of the IEEE. The research activities and interests of Prof. Gaillardon are currently focused on the development of reconfigurable logic architectures and digital circuits exploiting emerging transistor and memory technologies.

COFFEE BREAK
15.00 - 15.30

TITASH RAKSHIT
15.30 - 16.30

Spintronics in the context of computation

Abstract
In this lecture, I'll present an overview of spintronics in the context of computation. Spintronics holds promise of harnessing both charge and spin degrees of freedom of electrons. Advancements in logic transistors and memories, the key cogs of modern computation, in the past have been limited to the technological revolutions of electronic charge based systems. However, recent advances in the ability to control and manipulate electron spin have opened up the possibility to extend and add to this charge based computing paradigm. In this lecture, first I will briefly outline the history and the recent advances in the area of spintronics. Next, I will focus on how small dimensions, enabled by state-of-the-art lithography, have helped bring semiconductor spintronics closer to relevance at the level of a microprocessor. Then I'll discuss if and how manipulation and engineering of spin can help advance the current state-of-the-art von-Neumann architecture of a microprocessor. Possible other emergent computing paradigms enabled by spintronics will be covered briefly as well.

Bio
Titash Rakshit is a Principal Engineer at Samsung's Advanced Logic Lab. He received his PhD degree from Purdue University in 2004, in the area of Nanoelectronics. His thesis involved predicting negative differential resistance at the semiconductor-molecule interfaces. After graduation, he worked at Intel Corp. where he was involved with the industry first demonstration of a scaled finFET technology. Since 2014, he has been working at Samsung Advanced Logic Lab focusing on future technology and systems roadmap.

RONALD HANSON
16.30 - 17.30

Introduction to quantum computing

Abstract
Quantum computers could tackle problems in materials science, chemistry and mathematics that are well beyond the reach of supercomputers. Their power derives from the use of quantum bits, which can exist in arbitrary combinations of 0 and 1. This leads to a computing power that doubles with every additional quantum bit. The challenge is that quantum bits are extremely fragile and their state is easily perturbed by environmental fluctuations. Recent theoretical and experimental advances have made it clear that the resulting errors can in principle be corrected. This talk will introduce the basic concepts behind quantum computing, summarize the state-of-the-art of solid-state implementations of quantum circuits, and present the major open challenges in the realization of large-scale quantum circuits.

Bio
Ronald Hanson (Groningen, 1976) obtained his MSc degree in Applied Physics at the University of Groningen, whereafter he spent a year in Japan on a program run by the Dutch government to "educate and train future leaders of Dutch society" on interactions with Japan.
Ronald finished his PhD in Physics at TU Delft on Electron spins in semiconductor quantum dots. After being a postdoctoral researcher in both Delft and at the University of California in Santa Barbara, he was appointed 'Antoni van Leeuwenhoek Professor' at the TU Delft in 2012. His expertise lies in quantum optics and quantum information science, controlling single quantum objects in solids, single electrons in quantum dots and single spins and single photons using diamond NV centers. Ronald is fascinated by the concept that the world we live in has these strange properties such as being in two places at the same time and being entangled with something else. He devotes his time thinking about/working on making real-life technologies based on these bizarre phenomena
In the past, Ronald and his group managed to realize entanglement between two electrons at a 3 meter distance. This achievement brings him one step closer to one of his goals: secure communication over the web, also dubbed Quantum internet. In the coming years he would like to demonstrate the building blocks of a future quantum internet and of a future quantum computer, by using his unique quantum toolbox.

All tutorials will be held on Monday 11 September.
08.00 - 08.30 Registrations

- SENSORS FOR THE IOT ERA -

Tutorial Organizer: Mirjana Banjevic, Sensirion AG
Room **AV 02.17**

MIRJANA BANJEVIC

08.30 - 09.00

Introduction and Overview

Abstract

Sensors and sensor networks are getting increasingly more important in this era of connected 'things' ('Internet of Things' (IoT)). The sensor development will focus on the key business and technology markets related to healthcare, energy and environment to imagine and create a better future world. The tutorial will cover sensor technology and sensor systems for different application field in the IoT era. The focus will be on environmental monitoring, health monitoring and sensing for automotive applications. Environmental sensors hold promise for monitoring of environmental parameters such as temperature and concentration of hazardous gases with the aim of smart regulation for energy savings or life protection. As a result, this family of sensor lends itself to easy integration in IoT ecosystems. The current challenge on the sensor level is reduction of power consumption, both that of the sensor element and the signal processing electronics. Wearable sensors for health monitoring have a mission to enable diagnosing, monitoring, and treating various medical conditions. The goal is to create completely autonomous devices invisible to the user by making them thin and flexible in form, while keeping them efficient in power consumption both for data processing and data transmission. Sensors for automotive industry witness more stringent specifications by the day not only in performance, but also in terms of stability and robustness. In order to respond to the ever-raising bar for the automotive sensor specifications, the system level approach including chip design, packaging and calibration has been developed, the examples of which will be discussed in the session.

Bio

Mirjana Banjevic received M.Sc. Degree in Electronics from the School of Engineering, Montenegro, 2006, and PhD Degree in Microelectronics and Microsystems from Ecole Polytechnique Fédérale de Lausanne, EPFL, in 2011 in the field of magnetic sensors based on Hall devices. From 2012 till now she has been with Sensirion AG, Zürich, R&D department, working primarily on the novel integrated gas sensors. Her research and development interests are semiconductor physics, low power sensor interface electronics, analog building blocks and power management units. She has been a member of the ESSDERC Technical Program Committee, IEDM Technical Program Committee 2015-2016, and ISCAS 2017 reviewer.

FLORIN UDREA
09.00 - 10.00

Smart Sensors for Environmental Monitoring

Abstract
Environmental Smart Sensors are a new class of gas sensors that aim to replace the traditional chemical sensors such as those based on electrochemical or catalitic effects. They feature small form facor, very low power consumption, smart on-chip or on-package electronics and additional humidity and thermal sensors to compensate for undesirable factors such as humidity or temperature. Such sensors aim to detect voltalile organic compounds, NO, NO2, ozone, CO and other toxic gases.
CMOS technology is employed to manufacture such sensors in high volume at low unit cost. Their applications range from esatblished markets such as medical and automotive to new markets in cosnumer sector such as smart phones, watches, tablets, accessories and devices in smart homes.

Bio
Florin Udrea is a professor in semiconductor engineering and head of the High Voltage Microelectronics and Sensors Laboratory at University of Cambridge. He received the diploma of Engineering from Politehnica University of Bucharest, the MSc in smart sensors from the University of Warwick, UK, in 1992 and the PhD degree in power devices from the University of Cambridge, Cambridge, UK, in 1995. Since October 1998, Prof. Florin Udrea has been an academic with the Department of Engineering, University of Cambridge, UK.. He is currently leading a research group in power semiconductor devices and solid-state sensors that has won an international reputation during the last 20 years. Prof. Udrea has published over 450 papers in journals and international conferences. He holds more than 80 patents in power semiconductor devices and sensors. Prof. Florin Udrea co-founded five companies, Cambridge Semiconductor (Camsemi) in power ICs, Cambridge CMOS Sensors (CCS) in the field of smart sensors and Cambridge Microelectronics in Power Devices, Cam GaN Devices and Flusso in flow sensors. Camsemi was acquired by Power Integrations, US and CCS was acquired by ams, the latter being considered one of the best exits from Cambridge University in physical sciences For his 'outstanding personal contribution to Engineering', Prof Florin Udrea was awarded the Silver Medal (2012) from Royal Academy of Engineering. He is a board director of Cambridge Enterprise and from 2015 a fellow of Royal Academy of Engineering.

COFFEE BREAK
10.00 - 10.30

PATRICK MERCIER
10.30 - 11.30

Sensors for Health Monitoring

Abstract
Wearable devices hold considerable promise to diagnose, monitor, and treat various medical conditions and/or track the real-time status of athletes. However, most current generation wearable devices only monitor a limited number of physical and electrophysiological parameters that are, in many cases, only peripherally related to many health conditions or fitness enterprises. Furthermore, many such wearable devices are large, bulky, and rigid, thereby precluding seamless integration into daily life. Addressing these issues requires: 1) development of new sensor technologies that provide more actionable data in thin, flexible form factors, and 2) engineering of supporting electronic infrastructure to condition, digitize, and transmit data in an extremely energy efficient manner. This tutorial will discuss emerging sensor technologies that can non-invasively monitor physiochemistry (e.g., glucose, blood alcohol concentration, and lactate) in thin, flexible, wearable devices. We will also cover integrated circuit building blocks and architectures that make acquisition and telemetry of sensed information so energy-efficient that that they can be easily powered from new local energy sources (e.g., wearable glucose biofuel cells). Such net-zero-power operation will ultimately enable devices that are completely autonomous and invisible to the user, to the point where users are virtually unaware of their wearable devices after placement – in other words, they are "unawearable" devices.

Bio
Patrick Mercier is an Assistant Professor of Electrical and Computer Engineering and co-founder/co-director of the Center for Wearable Sensors at UC San Diego. He received his B.Sc. degree from the University of Alberta, Canada, in 2006, and the S.M. and Ph.D. degrees from MIT in 2008 and 2012, respectively. Prof. Mercier has received numerous awards, including the UCSD Academic Senate Distinguished Teaching Award in 2016, the DARPA Young Faculty Award in 2015, the Beckman Young Investigator Award in 2015, and the International Solid-State Circuits Conference (ISSCC) Jack Kilby Award in 2010. He is an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems, is a member of the ISSCC International Technical Program Committee, and has co-edited two books: Power Management Integrated Circuits (CRC Press, 2016), and Ultra-Low-Power Short-Range Radios (Springer, 2015). His research interests include the design of energy-efficient mixed-signal systems, RF circuits, power converters, and sensor interfaces for wearable, medical, and mobile applications.

APPO VAN DER WIEL
11.30 - 12.30

Sensors for Automotive Industry

Abstract
The requirements for sensors used for automotive applications get tougher every year. This does not only count for requirements in performance but especially for stability and robustness. System integration is key to meeting such future requirements. In the past, the sensor, interface circuit and package were developed independently of each other, whereas today performance has to be defined on system level, where package design and calibration methods have to be taken into account. Such a system level approach requires new methods for performance simulation and reliability testing. The tutorial will give a framework and several examples for this approach.

Bio
Appo van der Wiel was born in Ede, the Netherlands, in 1964. He received his M.Sc. Degree in Electronics from Twente University, the Netherlands, in 1990 on automation of bipolar analog design. He obtained PhD Degree in Microtechnology from University of Neuchatel, Switzerland in 1994 on silicon flow meters. His professional experiences includes: MEMS process flow owner at CSEM in Neuchatel Switzerland from 1995 to 2000, wafer level packaging at CS2 in collaboration with imec from 2000 to 2002 with focus on industrialization, and MEMS design and process definition for MEMS and wafer level packaging at Melexis from 2002 till now. His main professional interest is to bridge the world of microsystem design and microsystem fabrication using standard CMOS and standard packaging technology.

LUNCH
12.30 - 13.30

All tutorials will be held on Monday 11 September.

NEUROMORPHIC COMPUTING WITH EMERGING SYNAPTIC DEVICES

Tutorial Organizer: Shimeng Yu, Arizona State University

Room **AV 02.17**

SHIMENG YU

13.30 - 14.00

Neuro-inspired Computing using Resistive Synaptic Devices: Challenges and Prospects

Abstract

This tutorial introduces the recent breakthroughs in hardware implementation of neuro-inspired computing using resistive synaptic devices. The overview summarizes state-of-the-art, challenges and prospects of the neuro-inspired computing with emerging synaptic devices. First, we discuss the demand for developing neuro-inspired architecture beyond today's von-Neumann architecture. Second, we summarize the various approaches to designing the neuromorphic hardware (digital vs. analog, spiking vs. non-spiking, online training vs. offline training) and discuss why emerging non-volatile memory is attractive for implementing the synapses in the neural network. Then, we discuss the desired device characteristics of the synaptic devices (e.g. multilevel states, weight tuning linearity, variation/noises), and surveyed a few representative material systems and device prototypes reported in the literature that shows the analog conductance tuning. Next, we introduce the crossbar array architecture to efficiently implement the weighted sum and weight update operations that are commonly used in the neuro-inspired learning algorithms, and review the recent progresses of array-level experimental demonstrations for pattern recognition tasks. In addition, we discuss the peripheral neuron circuit design issues and present a device-circuit-algorithm co-design methodology to evaluate the impact of non-ideal device effects on the neuromorphic system performance (e.g. learning accuracy).

Bio

Shimeng Yu received the B.S. degree in microelectronics from Peking University, Beijing, China in 2009, and the M.S. degree and Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA in 2011, and in 2013, respectively. He is currently an assistant professor of electrical engineering and computer engineering at Arizona State University, Tempe, AZ, USA. His research interests are emerging nano-devices and circuits with a focus on the resistive memories for different applications including brain-inspired neuromorphic computing, hardware security, monolithic 3D integration, and radiation-hard electronics, etc. He has published >50 journal papers and >90 conference papers with citations >4000 and H-index 28. Among his honors, he is a recipient of the Stanford Graduate Fellowship from 2009 to 2012, the IEEE Electron Devices Society Masters Student Fellowship in 2010, the IEEE Electron Devices Society PhD Student Fellowship in 2012, the DOD-DTRA Young Investigator Award in 2015, and the NSF Faculty Early CAREER Award in 2016.

HYUNSANG HWANG
14.00 - 15.00

Analog Synapse Devices based on Interface Resistive Switching for Neuromorphic Systems

Abstract
Hardware artificial neural network (ANN) system with high density synapse and neuron can perform massive parallel computing which is effective for pattern recognition and clustering of unstructured data. To implement neuromorphic system, we need to develop ideal synapse device with various requirements such as scalability, MLC characteristics, low power operation, data retention, and symmetric potentiation/depression characteristics. Although various devices such as filamentary ReRAM, PRAM, and MRAM were proposed for synapse applications, these devices cannot meet the requirements of synapse device. Using redox reaction at metal/oxide interface, we developed analog synapse device. Compared with filament switching device which has intrinsic variability of switching parameters, interface resistive switching device exhibits excellent switching uniformity and area scalability. By controlling the reactivity of metal electrode and oxygen concentration in oxide, we can modulate conductance under potentiation and depression conditions. We have fabricated wafer-scale high density synapse array device with excellent switching uniformity. By modulating the linearity and symmetry of conductance change, we have estimated the accuracy of pattern recognition of handwritten digits. We found that synapse device with linear and symmetric conductance change exhibits improved pattern recognition accuracy.

Bio
Hyunsang Hwang is a professor in Pohang University of Science and Technology, department of Materials science and Engineering. In 1992, he graduated in Materials Science and Engineering from University of Texas at Austin. He worked as Principal Research Engineer, LG Semiconductor Company, Korea from 1992 to 1997. In 1997 he was appointed as a professor in Dept. of MSE, GIST, during this period, he worked as Visiting Research Professor in Department of Electrical Engineering in Stanford University, USA (2007~2008) and Oak Ridge National Lab., USA in 2002. In 2012 he leaved for Department of MSE in POSTECH as a professor. Until now, he has cultivated 23 Ph.D and 54 Master students, and 14 of them got the best student paper awards. He is author of about 330 journal papers and inventor of 55 international patents. During his career he has given 35 invited presentations, plenary talks and tutorial lectures. He is a Senior Member of IEEE Electron Device Society. He has been member of committees on important conferences such as IEEE International Electron Device Meeting (Memory Technology Program committee 2009, 2010), IEEE Semiconductor Interface Specialists Conf., (Technical Program Committee 2008, 2009, 2010) and International Conf. on Solid State Devices and Materials (program committee 2005-2008, 2011-2014). He also served as Technical Program Co-chair (2012) and Technical Program Vice-chair (2011) of Korean Conference on Semiconductors (KCS) and Chair of Thin Film committee (2009-2011).

COFFEE BREAK
15.00 - 15.30

DMITRI STRUKOV
15.30 - 16.30

Emerging Memories for Neurocomputing

Abstract
The present-day revolution in deep learning was triggered not by any significant algorithm breakthrough, but by the use of more powerful GPU hardware. Though this revolution has stimulated the development of even more powerful dedicated digital circuits, their speed and energy efficiency are still inadequate for more ambitious cognitive tasks and/or systems with severely limited power budget. On the other hand, the network performance may be dramatically improved using mixed-signal integrated circuits based on emerging nonvolatile memories, where the key inference-stage operation, the vector-by-matrix multiplication, is implemented on the physical level by utilization of the fundamental physical laws. In my talk I will review the recent progress of such mixed-signal neuromorphic networks based on two types of memory technologies – floating-gate memories and memristive arrays (also known as ReRAM). In particular, a minor modification of a highly optimized embedded NOR flash memory has already enabled a successful demonstration of the first 180-nm medium-scale network for pattern classification. The experimentally measured delay and energy dissipation per inference were at least three orders of magnitude better than those reported for digital implementation of the same task, with a similar fidelity. The detailed estimates show that the transfer to the similar 55 nm technology will allow the implementation of much larger networks, keeping a similar performance lead over the most prospective digital networks. Another way toward further scaling down of the mixed-signal neuromorphic networks is provided by novel nonvolatile two-terminal devices - memristors, which may have a sub-10-nm footprint, and are suitable for 3D integration. My group has developed a new technology of fabrication of these devices, sufficiently reproducible to demonstrate the first simple integrated neuromorphic networks. I will conclude my talk with a summary of challenges and future work, specific to the discussed devices and their applications.

Bio
Dmitri ("Dima") Strukov is an Associate Professor of Electrical and Computer Engineering at University of California at Santa Barbara. Prior to joining UCSB, Dmitri worked as a postdoctoral associate at Hewlett Packard Laboratories (Jan. 2007 – Jun. 2009) on various aspects of nanoelectronic systems. He received a MS in applied physics and mathematics from the Moscow Institute of Physics and Technology in 1999 and a PhD in electrical engineering from Stony Brook University in New York in 2006. He is a member of ACM, MRS, and IEEE societies. Dmitri's research broadly concerns different aspects of computation, in particular addressing questions on how to efficiently perform computation on various levels of abstraction. His current research focus is on hardware implementations of artificial neural networks with emerging memory devices.

GEOFFREY BURR

16.30 - 17.30

Accelerating Backpropagation Training with Non-Volatile Memory: Devices, Circuits and Architecture

Abstract

The scaling of traditional Von-Neumann computing has led us to systems with billions of devices that all have to work perfectly correctly, all the time. Scaling of future systems performance, in an era where device scaling is both slower and a less reliable source of performance scaling, may require systems that can still function without perfection on such enormous scales. Neuromorphic computation emulates the massive interconnectivity of the neurons and synapses found in the human brain. This effectively allows Deep Neural Networks to "throw too many resources" at problems, yet obtain useful results even in the presence of imperfect and noisy computing elements. I will review recent work in our field towards the development of neuromorphic chips that incorporate some form of analog non-volatile memory for hardware acceleration of the backpropagation training of Deep Neural Networks (DNNs), as well as forward-inference of already-trained networks. The requirements for devices, circuits, architecture and applications -- as well as the tradeoffs between these aspects -- will be discussed.

Bio

Geoffrey W. Burr received his Ph.D. in Electrical Engineering from the California Institute of Technology in 1996. Since that time, Dr. Burr has worked at IBM Research--Almaden in San Jose, California, where he is currently a Principal Research Staff Member. He has worked in a number of diverse areas, including holographic data storage, photon echoes, computational electromagnetics, nanophotonics, computational lithography, phase-change memory, storage class memory, and novel access devices based on Mixed-Ionic-Electronic-Conduction (MIEC) materials. Dr. Burr's current research interests include non-volatile memory and cognitive computing. An IEEE Senior Member, Geoff is also a member of MRS, SPIE, OSA, Tau Beta Pi, Eta Kappa Nu, and the Institute of Physics (IOP).

All workshops will be held on Monday 11 September.

CONNECT

Room **AV 04.17**

Abstract

The workshop will provide technical information about emerging interconnect technologies, with the focus on Carbon Nanotubes (CNT). A broad overview of all the major aspects of CNT interconnects will be offered, ranging from the innovative growth/deposition techniques of local and global lines to the novel measurement and simulation methodologies developed to characterize CNT performances. The core of the workshop will be based on the latest results arising from the research within the H2020 EU-funded project CONNECT. Invited talks from academia, research centers and industry will enrich the global perspective of the workshop.

Target Audience

The target audience is students, researchers, engineers and entrepreneurs who have an interest or work in the areas related to advanced and future interconnects for integrated circuits. Since interconnects delay is a major limitation to circuits performance, anyone interested in advanced CMOS technologies will benefit from the topics addressed by the workshops' talks. Researchers working in the field of Carbon Nanotubes, even if not for with direct application in interconnects technology, will also find cross-disciplinary interest in this workshop. Finally, CMOS circuit designers will be able to gather useful information on modeling, design and optimization opportunities offered by Carbon Nanotubes based technologies.

Background on CONNECT Project CarbON Nanotube compositE InterconneCTs

As the chip size goes down, interconnects become major bottlenecks irrespective of the application domain due to electromigration issues and an ever-increasing power consumption. The CONNECT project investigates ultra-fine CNT lines and metal- CNT composite material for addressing the issues of current state-of-the-art copper interconnects. Novel CNT interconnect architectures for the exploration of circuit- and architecture-level performance and energy efficiency will be developed. CMOS compatibility as well as challenges of transferring new processes into industrial mass production will be addressed. The members of the CONNECT consortium from Germany, Switzerland, Great Britain and France are embedded along the electronics value chain from fundamental research to end-users and bring together some of the most renowned research groups in that field in Europe. With significantly improved

electrical resistivity, ampacity, thermal and electromigration properties of CNT interconnects compared to state-of-the-art approaches for conventional copper interconnects, an increased power and scaling density of CMOS or CMOS extension will be available and applicable to alternative computing schemes such as neuromorphic computing. The technologies developed in this project are key for both performance and manufacturability of scaled microelectronics to manifest miniaturized microelectronic products with enhanced functionality at ever decreasing cost. The procurement of CONNECT will foster the recovery of market shares of the European electronic sector and prepare the industry for future developments of the electronic landscape. You can find more information about CONNECT project at the website www.connect-h2020.eu.

Program

8.00	Arrival & Registration
8.30	**Welcome and CONNECT Open Day Introduction** Prof. Aida Todri-Sanial, Dr. Salvatore M. Amoroso (Organizers)
8.45	**Overview of the EC H2020 CONNECT project** Dr. Benjamin Uhlig(Fraunhofer-Dresden)
9.00	**Highly Energy-Efficient Digital NanoSystems: New Logic, Memory, Interconnects, & 3D integration** Dr. Gage Krieger Hills (Stanford University)
9.35	**Direct, dry deposition of high quality SWNT thin films** Prof. Esko Kauppinen (Aalto University)
10.10	Coffee Break
10.40	**Doped CNTs for advanced local interconnects** Dr. Jean Dijon (CEA-Grenoble)
11.15	**CNT-metal-composites for global interconnects** Dr. Benjamin Uhlig (Fraunhofer-Dresden)
11.50	**Vertical Multi-walled CNT interconnects evaluation at full wafer level** Dr. Marleen van der Veen(imec)
12.30	Lunch Break
14.00	**Heterogeneous integration of low-dimensional nanomaterials** Dr. Shu-Jen Han(IBM TJ Watson)
14.35	**Manufacturability of CNT interconnects** Dr. Bingan Chen (AIXTRON-UK)
15.10	Coffee Break
15.40	**Thermal and Electrical Characterization of CNTs interconnects** Dr. Bernd Gotsmann (IBM-Zurich)
16.15	**Hierarchical multi-physics simulation of CNT interconnects** Prof. Aida Todri-Sanial (CNRS-Montpellier)
16.50	Wrap Up & Closure

All workshops will be held on Monday 11 September.

MOS-AK
Modeling of Systems and Parameter Extraction Working Group
Room **AV 91.12**

The MOS-AK is a HiTech forum to discuss the frontiers of electron device modeling with emphasis on simulation-aware models. The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

WWW.MOS-AK.ORG/LEUVEN_2017

Extended MOS-AK Committee
International MOS-AK Board of R&D Advisers
- Larry Nagel, Omega Enterprises Consulting (US)
- Andrei Vladimirescu, UCB (US); ISEP (FR)

MOS-AK Workshop Program Coordination
- Jean-Michel Sallese, EPFL (CH)
- Daniel Tomaszewski, ITE (PL)
- Wladek Grabinski, MOS-AK (EU)

MOS-AK Technical Committee
- www.mos-ak.org/committee.html

Program

8.00	Arrival & Registration
8.30	MORNING SESSIONS • **ASCENT: Access to Leading European Nanoelectronics Technology** Jim Greer, Tyndall (IRL) • **Junctionless Nanowire Transistors Performance: Static and Dynamic Modeling** Marcelo Pavanello, FEI (BR)
10.00	Coffee Break
10.30	MORNING SESSIONS (continued) • **Modeling and Analysis of Full-Chip Parasitic Substrate Currents** Wim Schoenmaker, Magwel (B) • **Small- and large-signal RF modeling of silicon-based substrates** Jean-Pierre Raskin, UCL (B) • **Spice modeling of beyond CMOS** Chika Tanaka, Toshiba (J)
12.30	Lunch
14.00	AFTERNOON SESSIONS • **ASCENT Open Access to 14nm PDKs** Nicolas Cordero, Tyndall (IRL) • **Modelling of Surface Traps Effect on Semiconductor Nanowires** Ashkhen Yesayan, IRPhE (AM)
15.00	Coffee Break
15.30	AFTERNOON SESSIONS (continued) • **Measurement and modelling of specific behaviors in 28nm FD SOI UTBB MOSFETs of importance for analog / RF amplifiers** Denis Flandre, UCL (B) • **IEEE EDS Compact Model Standardization** Benjamin Iniguez URV (SP) • **3D electromagnetic simulation and QUCS modeling of split ring resonators** Saravana Maruthamuthu, QUCS (D)
17.00	Closure

All workshops will be held on Monday 11 September.

SEMICONDUCTOR MEMORIES: the follow-up of a successful story

Room **AP 01.30**
(Auditorium Jean Monnet)

Organizer

Prof. Francisco Gamiz
Universidad de Granada & REMINDER Project

Abstract

In 1968, Dr.Robert Dennard from IBM introduced the concept of Dynamic Random Access Memory (DRAM) cell, which consists in a transistor (1T) and a capacitor (1C) where the information is stored. Since its introduction almost 50 years ago, this memory cell has been present in all electronic devices up to now. However, the arrival of the Internet of Things (IoT) and the requirement of ultra-low power consumption and extremely cheap devices are making developers to reconsider their design goals, by using memory in new and innovative ways. In many cases, this involves using new, or less familiar, memory technologies and examining memory much earlier in their design cycles. The vast majority of embedded memories are currently charged based (DRAM, FLASH) or flip-flop based (SRAM), the last one penalized by its huge area consumption. The other alternative storage options (which are not yet mature from and commercial perspective) can be grouped into three categories, ReRAM (resistive) or MRAM (magnetic), and body-charged memories (so called floating-body DRAMs, FB-DRAM). All these memory approaches will be analyzed by well-known experts in the field both from Industry and Academia.

Program

8.30	**Welcome Introduction** Prof. Francisco Gamiz (Unversidad de Granada, REMINDER project)
9.00	**MRAM solutions** Dr. Kilho Lee (MRAM Team, Samsung Electronics, Korea)
9.45	**FDX12 technology and embedded NVM solutions for IoT** Dr. Manfrest Horstman (Global Foundries, Dresden, Germany)
10.30	**Resistive memories for spike-based neuromorphic circuits** Dr. Elisa Vianello (CEA, France)
11.15	Coffee Break
11.45	**Stand-alone DRAM memory status and challenges** Dr. Pierre Fazan (Micron Europe, Leuven, Belgium)
12.30	**MRAM developments at IBM** Dr. Guohan Hu (IBM Yorktown Heights, New York, USA)
13.15	Lunch
14.30	**FDSOI technology for IoT applications** Dr. Philippe Galy (STMicroelectronics)
15.00	**Z2FET memory for low-power applications** Prof. Sorin Cristoloveanu (IMEP-MINATEC, Grenoble France)
15.30	**Modelling of Z2FET memory cell** Dr. Joris Lacord (CEA-LETI, Grenoble)
16.00	Coffee Break
16.30	**Variability of Z2FET memory cells and matrix** Prof. Asen Asenov (Glasgow and Synopsys U.K.)
17.00	**Circuit \design with Z2FET memory cell for low-power applications** Dr. Andy Pickering (Surecore U.K.)
17.30	Conclusions

All workshops will be held on Monday 11 September.

SINANO-NEREID
Towards a new NanoElectronics Roadmap for Europe

Room **AP 00.15**
(Auditorium Max Weber)

Organizers

Francis Balestra, Grenoble INP-CNRS (NEREID Coordinator), Enrico Sangiorgi, SiNANO Institute/IUNET (SINANO Institute Director), Ralf Popp, Edacentrum (NEREID Dissemination Manager)

Abstract

Within this Workshop the H2020 Coordination and Support Action NEREID entitled "NanoElectronics Roadmap for Europe: Identification and Dissemination" (https://www.nereid-h2020.eu/, n° 685559) will report on its recent findings on the way to map the future of European Nanoelectronics. The objective of this 3 year project NEREID is to elaborate a new NanoElectronics Roadmap for Europe using a pretty new method: starting from the needs of applications and leveraging the strengths of the European eco-system the advanced design and technology concepts are examined with respect to their potential to serve future application needs and/or to lead to possible disruptive applications. Focusing on a longer term time horizon, NEREID will lead to an application oriented early benchmark/identification of promising novel nanoelectronic technologies, and an identification of bottlenecks all along the innovation (value) chain.

In this workshop, which is supported by the European Institute of Nanoelectronics SINANO (www.sinano.eu) the NEREID project will report on its recent findings and will bring them into a hopefully vivid feedback situation with the audience, aiming to verify the current results by discussing especially controversial points. Besides applications like automotive, energy, health, IoT and many others, the topics of NEREID and the workshop comprise Beyond CMOS technologies, advanced logic and connectivity, functional diversification, system design and heterogeneous integration as well as equipment and manufacturing science.

Program

9.00	**Welcome** Enrico Sangiorgi (SINANO Institute)
9.05	**"Presentation of the NEREID Project"** Francis Balestra (Grenoble INP/CNRS)
9.25	**"European Status, Vision and Perspectives in Nanoelectronics"** Francisco Ibanez (European Commission)
10.00	**"Emerging technologies for Beyond CMOS"** Jouni Ahopelto (VTT)) **"Alternative Computing Paradigms"** Clivia Sotomayor Torres (ICN2)
10.45	Coffee Break
11.00	**"Advanced logic: Nanoscale FET"** Anda Mocuta (imec) **"RF and mmW Design/Connectivity"** Yann Deval (IMS Bordeaux)
11.45	**Functional Diversification:** **"Smart Sensors"** Montserrat Fernandez-Bolanos (EPFL) **"Smart Energy Devices"** Steve Stoffels (imec) **"Energy for Autonomous Systems"** Stéphane Monfray (ST Microelectronics)
12.45	Lunch
14.00	**"System Design"** Danilo Demarchi (Politechnico Di Torino) Holger Schmidt (Infineon) **"Heterogenous Integration"** Georgios Fagas (Tyndall)
14.45	**"Equipment and Manufacturing Science"** Thanasis Dimoulas (NCSRD)
15.30	**Conclusions** Enrico Sangiorgi (SINANO Institute)

Tuesday, September 12

Wednesday, September 13

Thursday, September 14

Tuesday, September 12

Joint Plenary 1: Françoise Chombar, Melexis - Engineering a Safe, Clean & Comfortable Future

Session Code: A1L-A
Location: Vesalius
Time: 09:00 - 09:40
Chair(s): Georges Gielen; *KU Leuven*

09:00 **Engineering a Safe, Clean & Comfortable Future**
Françoise Chombar
Melexis, Belgium

Joint Plenary 2: Peter Real, Analog Devices - Navigating without a Moore's Law Compass

Session Code: A2L-A
Location: Vesalius
Time: 09:40 - 10:20
Chair(s): Georges Gielen; *KU Leuven*

09:40 **Navigating Without a Moore's Law Compass**
Peter Real
Analog Devices Inc, Ireland

Tuesday, September 12

Resistive RAM

Session Code: A3L-F

Location: AP01.30

Time: 11:00 - 12:20

Chair(s): Thomas Mikolajick; *NaMLab gGmbH*
Paolo Pavan; *Università di Modena e Reggio Emilia*

11:00 **22% Higher Performance, 2x SCM Write Endurance Heterogeneous Storage with Dual Storage Class Memory and NAND Flash**
Chihiro Matsui, Ken Takeuchi
Chuo University, Japan

11:20 **Study of Error Repeatability and Recovery in 40nm TaOx ReRAM**
Takashi Inose[1], Seiichi Aritome[1], Ryutaro Yasuhara[2], Satoshi Mishima[2], Ken Takeuchi[1]
[1]Department of Electrical, Electronic, and Communication Engineering, Chuo University, Tokyo, Japan, Japan; [2]Panasonic Semiconductor Solutions Co., Ltd., 1 Kotari-yakemachi, Nagaokakyo, Kyoto, Japan, Japan

11:40 **Optimization of Writing Scheme on 1T1R RRAM to Achieve Both High Speed and Good Uniformity**
Shan Wang, Huaqiang Wu, Bin Gao, Ning Deng, Dong Wu, He Qian
Tsinghua University, China

12:00 **Analyzing Inference Robustness of RRAM Synaptic Array in Low-Precision Neural Network**
Rui Liu[1], Heng-Yuan Lee[2], Shimeng Yu[1]
[1]Arizona State University, United States; [2]Electronics and Optoelectronics Research Laboratory, Industrial Technology Research Institute, Taiwan

Tuesday, September 12

Cross-Domain Compact Modelling

Session Code: A3L-G

Location: AV00.17

Time: 11:00 - 12:20

Chair(s): Wladek Grabinski;
Cristell Maneux; *Laboratoire de l'Intégration du Matériau au Système*

11:00 **INVITED: SPICE Modeling in Verilog-A: Successes and Challenges**
Colin McAndrew
NXP Semiconductors, United States

11:40 **SPICE Modeling of Light Induced Current in Silicon with 'Generalized' Lumped Devices**
Chiara Rossi[2], Pietro Buccella[2], Camillo Stefanucci[1], Jean-Michel Sallese[2]
[1]AMS, AG, Schloss Premstaetten, Austria; [2]École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

12:00 **Total Ionizing Dose Effects on Analog Performance of 28 nm Bulk MOSFETs**
Chun-Min Zhang[3], Farzan Jazaeri[3], Alessandro Pezzotta[3], Claudio Bruschini[3], Gulio Borghello[2], Serena Mattiazzo[1], Andrea Baschirotto[4], Christian Enz[3]
[1]Department of Information Engineering, University of Padova, Italy; [2]EP-ESE Group, CERN and University of Udine, Switzerland; [3]Integrated Circuits Laboratory, École Polytechnique Fédérale de Lausanne, Switzerland; [4]Microelectronic Group, INFN Milano-Bicocca and University of Milano-Bicocca, Italy

Tuesday, September 12

Focus Session: Beyond CMOS Devices I

Session Code: A3L-H

Location: AV02.17

Time: 11:00 - 12:00

Chair(s): Joachim Knoch; *Rheinisch-Westfälische Technische Hochschule Aachen*
Thomas Zimmer; *Laboratoire de l'Intégration du Matériau au Système*

11:00 **1/f Noise in 3D Vertical Gate-All-Around Junction-Less Silicon Nanowire Transistors**
Chhandak Mukherjee[1], Julien Pezard[2], Guilhem Larrieu[2], Cristell Maneux[1]
[1]IMS Laboratory, University of Bordeaux, France; [2]LAAS-CNRS, Université de Toulouse CNRS, INP, Toulouse, France

11:20 **Random Telegraph Signal Noise in Tunneling Field-Effect Transistors with S Below 60 mV/decade**
Markus Hellenbrand, Elvedin Memišević, Johannes Svensson, Erik Lind, Lars-Erik Wernersson
Lund University, Sweden

11:40 **Experimental Characterization of the Static Noise Margins of Strained Silicon Complementary Tunnel-FET SRAM**
Gia Vinh Luong[1], Sebastiano Strangio[2], Andreas Tiedemann[1], Patrick Bernardy[1], Stefan Trellenkamp[1], Pierpaolo Palestri[2], Siegfried Mantl[1], Qing-Tai Zhao[1]
[1]Forschungszentrum Juelich, Germany; [2]University of Udine, Italy

Tuesday, September 12

Alternative Device Simulations

Session Code: A4L-F

Location: AP01.30

Time: 14:00 - 15:20

Chair(s): Francois Triozon; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Fabian Bufler; *Synopsys, Inc.*

14:00 **INVITED: Advances in the Understanding of Microscopic Switching Mechanisms in ReRAM Devices**
Benoît Sklénard[1], Philippe Blaise[1], Boubacar Traoré[2], Alberto Dragoni[1], Cécile Nail[1], Elisa Vianello[1]
[1]CEA LETI, France; [2]Institut des Sciences Chimiques de Rennes, France

14:40 **Modeling the Effect of Surface Roughness on the Performance of Line Tunnel Fets**
Saurabh Sant, Andreas Schenk
Integrated Systems Laboratory, ETH Zurich, Switzerland

15:00 **Material Selection and Device Design Guidelines for Two-Dimensional Material Based TFETs**
Tarun Agarwal[3], Bart Soree[3], Iuliana Radu[1], Praveen Raghavan[1], Gianluca Fiori[4], Marc Heyns[3], Wim Dehaene[2]
[1]imec, Belgium; [2]KU Leuven, Belgium; [3]KU Leuven/imec, Belgium; [4]Univ of Pisa, Italy

Tuesday, September 12

Parameter Extraction

Session Code: A4L-G

Location: AV00.17

Time: 14:00 - 15:20

Chair(s): Thierry Poiroux; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Marco Bellini; *ABB Group*

14:00 **Nanometer CMOS Characterization and Compact Modeling at Deep-Cryogenic Temperatures**
Rosario Marco Incandela[1], Lin Song[2], Harald Homulle[1], Fabio Sebastiano[1], Edoardo Charbon[1], Andrei Vladimirescu[1]
[1]Delft University of Technology, Netherlands; [2]Tsinghua University, China

14:20 **Cryogenic Characterization of 28 nm Bulk CMOS Technology for Quantum Computing**
Arnout Beckers[3], Farzan Jazaeri[3], Andrea Ruffino[1], Claudio Bruschini[2], Andrea Baschirotto[4], Christian Enz[3]
[1]EPFL AQUA, Switzerland; [2]EPFL AQUA-ICLAB, Switzerland; [3]EPFL ICLAB, Switzerland; [4]INFN Milano Bicocca, Italy

14:40 **A New Method for Junctionless Transistors Parameters Extraction**
Renan Trevisoli[2], Rodrigo Doria[2], Michelly de Souza[2], Sylvain Barraud[1], Marcelo Pavanello[2]
[1]CEA, LETI, Minatec Campus, France; [2]Centro Universitário FEI, Brazil

15:00 **Avalanche Compact Model Featuring SiGe HBTs Characteristics Up to BVCBO**
Mathieu Jaoul[5], Didier Céli[4], Cristell Maneux[3], Michael Schröter[2], Andreas Pawlak[1]
[1]Dresden University of Technology, Germany; [2]Dresden University of Technology, University of California, Germany; [3]IMS Bordeaux, France; [4]STMicroelectronics, France; [5]STMicroelectronics, IMS, France

Tuesday, September 12

Focus Session: Beyond CMOS Devices II

Session Code: A4L-H

Location: AV02.17

Time: 14:00 - 15:00

Chair(s): Joachim Knoch; *Rheinisch-Westfälische Technische Hochschule Aachen*
Thomas Zimmer; *Laboratoire de l'Intégration du Matériau au Système*

14:00 **Utilizing I-V Non-Linearity and Analog State Variations in ReRAM-Based Security Primitives**
Gina Cristina Adam[1], Hussein Nili[3], Jeeson Kim[2], Brian Douglas Hoskins[3], Omid Kavehei[2], Dmitri Strukov[3]
[1]National Institute for R&D in Microtechnologies, Bucharest, Romania; [2]RMIT University, Australia; [3]University of California Santa Barbara, United States

14:20 **Negative Capacitance Field Effect Transistors: Capacitance Matching and Non-Hysteretic Operation**
Ali Saeidi, Farzan Jazaeri, Francesco Bellando, Igor Stolichnov, Christian Enz, Adrian Ionescu
Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

14:40 **Buried Multi-Gate InAs-Nanowire FETs**
Thomas Grap, Felix Riederer, Charu Gupta, Joachim Knoch
RWTH Aachen, Germany

Tuesday, September 12

ESSDERC Keynote 1: Ian Young - Principles and Trends in Quantum Nano-Electronics and Nano-Magnetics for Beyond-CMOS Computing

Session Code: A5L-F

Location: AP01.30

Time: 15:50 - 16:30

Chair(s): Marc Heyns; *imec*

15:50 **Principles and Trends in Quantum Nano-Electronics and Nano-Magnetics for Beyond-CMOS Computing**
Ian A. Young, Dmitri E. Nikonov
Intel Corp., United States

Tuesday, September 12

Modelling of Emerging Devices

Session Code: A6L-G

Location: AV00.17

Time: 16:40 - 18:00

Chair(s): Jean-Michel Sallese; École polytechnique fédérale de Lausanne
Daniel Tomaszewski; *Institute of Electron Technology*

16:40 **Equivalent Circuit Model for the Electron Transport in 2D Resistive Switching Material Systems**
Enrique Miranda[2], Chengbin Pan[1], Marco Villena[1], Na Xiao[1], Jordi Suñe[2], Mario Lanza[1]
[1]Soochow University, China; [2]Universitat Autonoma de Barcelona, Spain

17:00 **Analytical Drain Current Model for Non-Ballistic Schottky-Barrier CNTFETs**
Igor Bejenari, Michael Schroter, Martin Claus
Technische Universitat Dresden, Germany

17:20 **A General Circuit Model for Spintronic Devices Under Electric and Magnetic Fields**
Meshal Alawein, Hossein Fariborzi
King Abdullah University of Science and Technology, Saudi Arabia

17:40 **Compact Physical Model of a-IGZO TFTs for Circuit Simulation**
Matteo Ghittorelli[3], Fabrizio Torricelli[3], Carmine Garripoli[2], Jan-Laurens van der Steen[1], Gerwin Gelinck[1], Sahel Abdinia[2], Eugenio Cantatore[2], Zsolt Kovàcs-Vajna[3]
[1]TNO, Netherlands; [2]Tu/e, Netherlands; [3]University of Brescia, Italy

Tuesday, September 12

2D Material Devices

Session Code: A6L-H

Location: AV02.17

Time: 16:40 - 18:00

Chair(s): Cees de Groot; *University of Southampton*
Gianluca Fiori; *Università di Pisa*

16:40 **Complementary Black Phosphorous FETs by Workfunction Engineering of Pre-Patterned Au and Ag Embedded Electrodes**
Nicolo Oliva, Emanuele Andrea Casu, Wolfgang Amadeus Vitale, Igor Stolichnov, Adrian Mihai Ionescu
EPFL, Switzerland

17:00 **Tunneling Transistors Based on MoS2/MoTe2 Van der Waals Heterostructures**
Yashwanth Balaji, Quentin Smets, Cesar J Lockhart de la Rosa, Anh Khoa Augustin Lu, Daniele Chiappe, Tarun Agarwal, Dennis Lin, Cedric Huyghebaert, Iuliana Radu, Dan Mocuta, Guido Groeseneken
imec, Belgium

17:20 **Temperature Dependence of Contact Resistance for Gold-Graphene Contacts**
Amit Gahoi, Satender Kataria, Max Christian Lemme
University of Siegen, Germany

17:40 **Radical Oxidation Process for Hybrid SAM/HfOx Gate Dielectrics in MoS2 FETs**
Takamasa Kawanago, Ryo Ikoma, Tomoaki Oba, Hiroyuki Takagi
Tokyo Institute of Technology, Japan

Wednesday, September 13

Joint Plenary 3: Hans Stork, ON Semiconductor - Smart Power for Automotives

Session Code: B1L-A

Location: Vesalius

Time: 08:45 - 09:25

Chair(s): Jo De Boeck; *imec*

09:00 **Smart Power for Automotives**
Johannes Stork
ON Semiconductor, United States

Wednesday, September 13

Widebandgap Power Devices

Session Code: B2L-F

Location: AP01.30

Time: 10:10 - 11:50

Chair(s): Mikael Ostling; *KTH Royal Institute of Technology*
Susanna Reggiani; *Università di Bologna*

10:10 **INVITED: CoolSiC(TM) and Major Trends in SiC Power Device Development**
Roland Rupp
Infineon Technologies AG, Germany

10:50 **Gated Base Structure for Improved Current Gain in SiC Bipolar Technology**
Gunnar Malm, Hossein Elahipanah, Arash Salemi, Mikael östling
KTH, Sweden

11:10 **On the Understanding of Cathode Related Trapping Effects in GaN-on-Si Schottky Diodes**
William Vandendaele, Thomas Lorin, Romain Gwoziecki, Yannick Baines, Jérome Biscarrat, Marie-Anne Jaud, Charlotte Gillot, Matthew Charles, Marc Plissonnier, Gilles Reimbold
CEA-LETI, France

11:30 **Temperature Dependent Substrate Trapping in AlGaN/GaN Power Devices and the Impact on Dynamic Ron**
Arno Stockman[2], Michael Uren[4], Alaleh Tajalli[5], Matteo Meneghini[5], Benoit Bakeroot[1], Peter Moens[3]
[1]CMST imec/Ghent University, Belgium; [2]Ghent University, Belgium; [3]ON Semiconductor, Belgium; [4]University of Bristol, United Kingdom; [5]University of Padova, Italy

Wednesday, September 13

Advanced CMOS Characterization and Reliability

Session Code: B2L-G

Location: AV00.17

Time: 10:10 - 12:10

Chair(s): Erik Bury; *imec*
Maryline Bawedin; *Minatec*

10:10 **INVITED: Material and Device Innovation Impact on Reliability for Scaled CMOS Technologies**
Tanya Nigam, Andreas Kerber, Tian Shen, Rakesh Ranjan, Linjun Cao
GLOBALFOUNDRIES, United States

10:50 **Carrier Lifetime Evaluation in FD-SOI Layers**
Kyung Hwa Lee, Maryline Bawedin, Hyungjin Park, Mukta Singh Parihar, Sorin Cristoloveanu
IMEP-LAHC, France

11:10 **Precise EOT Regrowth Extraction Enabling Performance Analysis of Low Temperature Extension First Devices**
Jessy Micout[2], Quentin Rafhay[3], Xavier Garros[1], Mikael Casse[1], Jean Coignus[1], Luca Pasini[1], Cao-Minh Vincent Lu[1], Nils Rambal[1], Claire Fenouillet-Beranger[1], Laurent Brunet[1], Giovanii Romana[4], Rémy Gassilloud[1], Perrine Batude[1], Maud Vinet[1], Gérard Ghibaudo[3]
[1]CEA-LETI, France; [2]CEA-LETI, IMEP-LAHC, France; [3]IMEP-LAHC, France; [4]STMicroelectronics, France

11:30 **Back-Gate Bias Effect on UTBB-FDSOI Non-Linearity Performance**
Babak Kazemi Esfeh[3], Valeria Kilchytska[3], Bertrand Parvais[1], N. Planes[2], M. Haond[2], Denis Flandre[3], Jean-Pierre Raskin[3]
[1]imec, Belgium; [2]ST-Microelectronics, France; [3]UCL, Belgium

11:50 **Evolution of Oxygen Vacancies Under Electrical Characterization for HfOx-Based ReRAMs**
Behnoush Attarimashalkoubeh, Jury Sandrini, Elmira Shahrabi, Yusuf Leblebici
Microelectronic Systems Laboratory (LSM),EPFL, Switzerland

Wednesday, September 13

Emerging Memory Technologies

Session Code: B2L-H
Location: AV02.17
Time: 10:10 - 12:10
Chair(s): Jerome Dubois; *NXP*
Dirk Wouters; *RWTH Aachen*

10:10 **INVITED: Emerging Memory Technologies for High Density Applications**
Giorgio Servalli
Micron Technology, Italy

10:50 **Anti-Ferroelectric ZrO2: An Enabler for Low Power Non-Volatile 1T-1C and 1T Random Access Memories**
Milan Pesic[2], Michael Hoffmann[2], Claudia Richter[2], Stefan Slesazeck[2], Thomas Kämpfe[1], Lukas Eng[1], Thomas Mikolajick[3], Uwe Schroeder[2]
[1]IAPP/TU Dresden, Germany; [2]NaMLab gGmbH, Germany; [3]NaMLab gGmbH/TU Dresden, Germany

11:10 **From Planar to Vertical Capacitors : a Step Towards Ferroelectric V-FeFET Integration**
Karine Florent[2], Simone Lavizzari[1], Luca Di Piazza[1], Mihaela Popovici[1], Goedele Potoms[1], Tom Raymaekers[1], Guido Groeseneken[2], Jan Van Houdt[2]
[1]imec, Belgium; [2]imec/KU Leuven, Belgium

11:30 **Doped GeSe Materials for Selector Applications**
Naga Sruti Avasarala[3], Bogdan Govoreanu[2], Karl Opsomer[2], Wouter Devulder[2], Sergiu Clima[2], Christophe Detavernier[1], Marleen van der Veen[2], Jan Van Houdt[3], Marc Heyns[3], Ludovic Goux[2], Gouri Sankar Kar[2]
[1]Ghent University, Belgium; [2]imec, Belgium; [3]imec, KU Leuven, Belgium

11:50 **Multilevel SOT-MRAM Cell with a Novel Sensing Scheme for High-Density Memory Applications**
Behzad Zeinali, Mahsa Esmaeili, Jens Kargaard Madsen, Farshad Moradi
Aarhus University, Denmark

Wednesday, September 13

ESSDERC Keynote 2: Siva Sivaram - Storage Class Memories: Desire Meets Reality

Session Code: B3L-F

Location: AP01.30

Time: 13:30 - 14:10

Chair(s): Bogdan Govoreanu; *imec*

13:30 **Storage Class Memories: Desire Meets Reality**
Siva Sivaram
Western Digital Corporation, United States

Wednesday, September 13

FinFET and Nanowire Simulations

Session Code: B4L-F

Location: AP01.30

Time: 14:20 - 15:40

Chair(s): Bernd Meinerzhagen; *TU Braunschweig*
Mathieu Luisier; *ETHZ*

14:20 **On the Ballistic Ratio in 14nm-Node FinFETs**
Fabian Bufler, Kenichi Miyaguchi, Thomas Chiarella, Naoto Horiguchi, Anda Mocuta
imec, Belgium

14:40 **Three-Dimensional Multi-Subband Simulation of Scaled FinFETs**
Luca Donetti, Carlos Sampedro, Francisco García Ruiz, Andrés Godoy, Francisco Gámiz
Universidad de Granada, Spain

15:00 **Study of Strained Effects in Nanoscale GAA Nanowire FETs Using 3D Monte Carlo Simulations**
Muhammad Elmessary[1], Daniel Nagy[2], Manuel Aldegunde[3], Antonio Garcia-Loureiro[2], Karol Kalna[1]
[1]Swansea University, United Kingdom; [2]Universidade de Santiago de Compostela, Spain; [3]University of Notre Dame, United States

15:20 **Investigation of Electrically Gate-All-Around Hexagonal Nanowire FET (HexFET) for 5nm Node Logic and SRAM Applications**
Jeffrey Smith[2], Kai Ni[2], Ram Krishna Ghosh[2], Jeff Xu[1], Mustafa Badaroglu[1], Pr Chidi Chidambaram[1], Suman Datta[2]
[1]Qualcomm, United States; [2]University of Notre Dame, United States

Wednesday, September 13

Traps and Noise

Session Code: B4L-G

Location: AV00.17

Time: 14:20 - 15:40

Chair(s): Benjamin Iniguez; *Universitat Rovira i Virgili*
Sadayuki Yoshitomi; *Toshiba*

14:20 **Modeling of Dynamic Trap Density Increase for Aging Simulation of Any MOSFET Circuits**
Mitiko Miura-Mattausch[3], Hidenori Miyamoto[3], Hideyuki Kikuchihara[3], Dondee Navarro[3], Tapas K. Maiti[3], Nezam Rohbani[4], Chenyue Ma[2], Hans Juergen Mattausch[3], Alexander Schiffmann[1], Alexander Steinmair[1], Ehrenfried Seebacher[1]
[1]ams, Austria; [2]ASTRI, Hong Kong; [3]Hiroshima University, Japan; [4]Sharif University, Iran

14:40 **Comprehensive Compact Electro-Thermal GaN HEMT Model**
Muhammad Alshahed, Mina Dakran, Lars Heuken, Mohammed Alomari, Joachim Burghartz
IMS CHIPS, Germany

15:00 **Trap-Assisted Carrier Transport Through the Multi-Stack Gate Dielectrics of HKMG nMOS Transistors: a Compact Model**
Apoorva Ojha, Nihar Ranjan Mohapatra
IIT Gandhinagar, India

15:20 **A New Verilog-A Compact Model of Random Telegraph Noise in Oxide-Based RRAM for Advanced Circuit Design**
Francesco Maria Puglisi, Nicolò Zagni, Luca Larcher, Paolo Pavan
Università di Modena e Reggio Emilia, Italy

Wednesday, September 13

2D Material Integration

Session Code: B4L-H

Location: AV02.17

Time: 14:20 - 15:40

Chair(s): Thomas Ernst; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Max Lemme; *Universität Siegen*

14:20 **INVITED: Ink-Jet Printed 2D Crystal Heterostructures**
Francesco Bonaccorso
Istituto Italiano di Tecnologia, Italy

15:00 **WS2 Transistors on 300 mm Wafers with BEOL Compatibility**
Tom Schram[2], Quentin Smets[2], Benjamin Groven[2], Markus Heyne[2], Eddy Kunnen[2], Arame Thiam[2], Katia Devriendt[2], Annelies Delabie[2], Dennis Lin[2], Marcel Lux[2], Daniele Chiappe[2], Inge Asselberghs[2], Stephan Brus[2], Cedric Huyghebaert[2], Safak Sayan[2], A. Juncker[1], Matty Caymax[2], Iuliana Radu[2]
[1]COVENTOR, France; [2]imec, Belgium

15:20 **200 mm Wafer Level Graphene Transfer by Wafer Bonding Technique**
Mesut Inac[1], Grzegorz Lupina[2], Matthias Wietstruck[2], Marco Lisker[2], Mirko Fraschke[2], Andreas Mai[2], Fabio Coccetti[3], Mehmet Kaynak[2]
[1]Berlin Technical University, Germany; [2]IHP, Germany; [3]RF Microtech, Italy

Thursday, September 14

Joint Plenary 4: Tetsuo Endoh, Tohoku University - Spintronics Applications: STT-MRAM & Non Volatile Logic

Session Code: C1L-A
Location: Vesalius
Time: 09:00 - 09:45
Chair(s): Jo De Boeck; *imec*

08:45 **Spintronics**
Tetsuo Endoh
Tohoku University, Japan

Thursday, September 14

Focus Session: Neuromorphic Computing

Session Code: C2L-E

Location: AV03.12

Time: 10:20 - 11:40

Chair(s): Cor Claeys; *imec*

10:20 **INVITED: Neuromorphic Computing: Architectures and Applications**
Karlheinz Meier
University of Heidelberg, Germany

11:00 **INVITED: RRAM: Does It Have the Potential for Neuromorphic Computation**
Praveen Raghavan
imec, Belgium

Thursday, September 14

Photonics / Microwave / Harsh Enviroment

Session Code: C2L-F

Location: AP01.30

Time: 10:20 - 12:00

Chair(s): Denis Flandre; *Université catholique de Louvain*
Dana Cristea; *IMT Bucharest*

10:20 **Epitaxial Growth and Diffusion Characteristics Analysis of Vertical Thin Poly-Si Channel Transfer Gate Structured Pixels for 3D CMOS Image Sensor**
Sung-Kun Park[2], Donghyun Woo[2], Min-Ki Na[2], Pyong-Su Kwag[2], Ho-Ryeong Lee[2], Kyoung-Wook Ro[2], Kyung-Hwan Kim[2], Dong-Kyu Lee[2], Chris Hong[2], In-Wook Cho[2], Kyung-Dong Yoo[1]
[1]Hanyang University, Korea; [2]SK hynix, Korea

10:40 **Modelling, Design and Characterization of Schottky Diodes in 28nm Bulk CMOS for 850/1310/1550nm Fully Integrated Optical Receivers**
Wouter Diels, Michiel Steyaert, Filip Tavernier
KULeuven, Belgium

11:00 **Importance of Buffer Configuration in GaN HEMTs for High Microwave Performance and Robustness**
Romain Pecheux, Riad Kabouche, Ezgi Dogmus, Astrid Linge, Etienne Okada, Malek Zegaoui, Farid Medjdoub
IEMN-CNRS, France

11:20 **Shunt Capacitive Switches Based on VO2 Metal Insulator Transition for RF Phase Shifter Applications**
Emanuele Andrea Casu, Wolfgang Amadeus Vitale, Michele Tamagnone, Mariazel Maqueda Lopez, Nicolò Oliva, Anna Krammer, Andreas Schüler, Montserrat Fernandez-Bolaños, Adrian Mihai Ionescu
EPFL, Switzerland

11:40 **Single Event Effects and Total Ionising Dose in 600V Si-on-SiC LDMOS Transistors for Rad-Hard Space Applications**
Khaled Ben Ali[3], Peter Gammon[4], Chunwa Chan[4], Fan Li[4], Vasantha Pathirana[1], Tanya Trajkovic[1], Farzan Gity[2], Denis Flandre[3], Valeriya Kilchytska[3]
[1]Cambridge Microelectronics Limited, United Kingdom; [2]Tyndall National Institute at University of Ireland, Ireland; [3]Université catholique de Louvain, Belgium; [4]University of Warwick, United Kingdom

Thursday, September 14

Advanced CMOS Technology

Session Code: C2L-G

Location: AV00.17

Time: 10:20 - 12:20

Chair(s): Francois Andrieu; *Commissariat à l'Energie Atomique et aux Energies Alternatives*
Blandine Duriez; *TSMC*

10:20 **PPAC Scaling Enablement for 5nm Mobile SoC Technology**
Mustafa Badaroglu[4], Jeff Xu[4], John Zhu[4], Da Yang[4], Jerry Bao[4], Sc Song[4], Peijie Feng[4], Romain Ritzenthaler[3], Hans Mertens[3], Geert Eneman[3], Naoto Horiguchi[3], Jeffrey Smith[5], Suman Datta[5], David Kohen[2], Po-Wen Chan[1], Keagan Chen[1], Chidi Chidambaram[4]
[1]Applied Materials, United States; [2]ASM International, Belgium; [3]imec, Belgium; [4]Qualcomm Technologies Inc., Belgium; [4]Qualcomm Technologies Inc., United States; [5]University of Notre Dame, United States

10:40 **INVITED: Hybrid InGaAs/SiGe CMOS Circuits with 2D and 3D Monolithic Integration**
Veeresh Deshpande, Herwig Hahn, Vladimir Djara, Eamon O'Connor, Daniele Caimi, Marilyne Sousa, Jean Fompeyrine, Lukas Czornomaz
IBM Research GmbH, Switzerland

11:20 **Tunable ESD Clamp for High-Voltage Power I/O Pins of a Battery Charge Circuit in Mobile Applications**
Mirko Scholz, Geert Hellings, Shih-Hung Chen, Dimitri Linten
imec, Belgium

11:40 **Guidelines for Intermediate Back End of Line (BEOL) for 3D Sequential Integration**
Claire Fenouillet-Beranger[1], Sylvain Beaurepaire[1], Fabien Deprat[1], Alexandre Ayeres de Sousa[1], Laurent Brunet[1], Perrine Batude[1], Paul Besombes[1], Marie-Pierre Samson[2], Fabrice Nemouchi[1], François Andrieu[1], Romain Famulok[1], Nils Rambal[1], Viorel Balan[1], Vincent Jousseaume[1], Vincent Delaye[1], Xavier Federspiel[2], Maud Vinet[1], O. Rozeau[1], B. Previtali[1], G. Rodriguez[1], P. Rodriguez[1], Z. Saghi[1], C. Guerin[1], F. Ibars[2], F. Proud[2], D. Nouguier[2], D. Ney[2], H. Dansas[1]
[1]CEA/LETI, France; [2]STMicroelectronics, France

12:00 **Device Circuit and Technology Co-Optimisation for FinFET Based 6T SRAM Cells Beyond N7**
Mohit Gupta[2], Pieter Weckx[1], Stefan Cosemans[1], Pieter Schuddinck[1], Rogier Baert[1], Dmitry Yakimets[1], Doyoung Jang[1], Yasser Sherazi[1], Praveen Raghavan[1], Alessio Spessot[1], Anda Mocuta[1], Wim Dehaene[2]
[1]imec, Belgium; [2]KU Leuven/imec, Belgium

Thursday, September 14

Microfluidics and TFTs

Session Code: C2L-H
Location: AV02.17
Time: 10:20 - 12:00
Chair(s): Montserrat Fernandez-Bolanos; École Polytechnique Fédérale de Lausanne
Joachim Burghartz; *IMS Chips*

10:20 **INVITED: Microfluidic Technology: New Opportunities to Develop Physiologically Relevant in vitro Models**
Séverine Le Gac
University of Twente, Netherlands

11:00 **Development of Ultrasensitive Extended-Gate Ion-Sensitive-Field-Effect-Transistor Based on Industrial UTBB FDSOI Transistor**
Getenet Tesega Ayele[3], Stephane Monfray[4], Frederic Boeuf[4], Jean-Pierre Cloarec[1], Serge Ecoffey[3], Dominique Drouin[3], Etienne Puyoo[2], Abdelkader Souifi[2]
[1]Ecole Central de Lyon, France; [2]INSA Lyon, France; [3]Sherbrooke University, Canada; [4]STMicroelectronics, France

11:20 **Ultrathin Lateral Unidirectional Bipolar-Type Insulated-Gate Transistor as pH Sensor**
Qinghua Han[1], Anran Gao[1], Keyvan Narimani[1], Yuelin Wang[2], Tie Li[2], Siegfried Mantl[1], Qing-Tai Zhao[1]
[1]Forschungszentrum Jülich, Germany; [2]Shanghai Institute of Microsystem and Information Technology, China

11:40 **A Novel Approach for Scalable Sensor Arrays Using Cantilever Field-Effect Transistors**
Andreas Hessel, Stefan Scholz, Alexander Pelger, Albert Pfander, Joachim Knoch
RWTH Aachen University, Germany

12:00 **ESD Characterization of a-IGZO TFTs on Si and Foil Substrates**
Nian Wang[3], Shih-Hung Chen[1], Geert Hellings[1], Kris Myny[1], Soeren Steudel[1], Mirko Scholz[1], Roman Boschke[2], Dimitri Linten[1], Guido Groeseneken[2]
[1]imec, Belgium; [2]imec, KU Leuven, Belgium; [3]KULeuven, imec, Belgium

Thursday, September 14

ESSDERC Keynote 3: David DiVincenzo - Control Systems for Quantum Computers

Session Code: C3L-F

Location: AP01.30

Time: 13:30 - 14:10

Chair(s): Guido Groeseneken; *imec*

13:30 **Control Systems for Quantum Computers**
David DiVincenzo
RWT Aachen, Germany

Thursday, September 14

Modelling and Measurement of Alternative Material Devices

Session Code: C4L-F

Location: AP01.30

Time: 14:20 - 15:40

Chair(s): Denis Rideau; *STMicroelectronics*
Massimo Rudan; *Università di Bologna*

14:20 **INVITED: Dopant Diffusion and Segregation, Si-Ge Interdiffusion and Defect Engineering in SiGe Devices**
Guangrui Xia
University of British Columbia, Canada

15:00 **Physical Modeling of the Hysteresis in MoS2 Transistors**
Theresia Knobloch[2], Gerhard Rzepa[2], Yury Yuryevich Illarionov[2], Michael Waltl[2], Franz Schanovsky[1], Markus Jech[2], Bernhard Stampfer[2], Marco Mercurio Furchi[3], Thomas Müller[3], Tibor Grasser[2]
[1]Global TCAD Solutions, Bösendorferstraße 1/12, 1010 Wien, Austria; [2]Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, 1040 Wien, Austria; [3]Institute for Photonics, TU Wien, Gußhausstraße 27–29/E387, 1040 Wien, Austria

15:20 **Impact of Impurities, Interface Traps and Contacts on MoS2 MOSFETs: Modelling and Experiments**
Gioele Mirabelli, Farzan Gity, Scott Monaghan, Paul Hurley, Ray Duffy
Tyndall National Institute, University College Cork, Ireland

Thursday, September 14

High Mobility Materials and Nanowires

Session Code: C4L-G

Location: AV00.17

Time: 14:20 - 15:40

Chair(s): Lukas Czornomaz; *IBM Zurich*
Nadine Collaert; *imec*

14:20 **Electron Mobility in Thin In0.53Ga0.47As Channel**
Eduard Cartier, Amlan Majumdar, Ko-Tao Lee, Takashi Ando, Martin M Frank, John Rozen, Keith A Jenkins, Cheng-Wei Cheng, John Bruley, Marinus Hopstaken, Pranita Kerber, Jeng-Bang Yau, Xiao Sun, Renee T Mo, Chun-Chen Yeh, Effendi Leobandung, Vijay Narayanan, C. Liang
IBM Corporation, United States

14:40 **Understanding of Slow Traps Generation in Plasma Oxidation GeOx/Ge MOS Interfaces with ALD High-K Layers**
Mengnan Ke, Mitsuru Takenaka, Shinichi Takagi
the University of Tokyo, Japan

15:00 **Isolation of Nanowires Made on Bulk Wafers by Ground Plane Doping**
Romain Ritzenthaler, Hans Mertens, An de Keersgieter, Jerome Mitard, Dan Mocuta, Naoto Horiguchi
imec, Belgium

15:20 **In-Depth Electrical Characterization of Carrier Transport in Ambipolar Si-NW Schottky-Barrier FETs**
Dae-Young Jeon[2], Tim Baldauf[5], So Jeong Park[3], Sebastian Pregl[4], Larysa Baraban[1], Gianaurelio Cuniberti[1], Thomas Mikolajick[4], Walter M. Weber[4]
[1]Institute for Materials Science and Max Bergmann Center of Biomaterials, Germany; [2]KIST, Jeonbuk, Korea; [3]Korea University, Korea; [4]Namlab gGmbH, Germany; [5]University of Applied Sciences Dresden, Germany

Thursday, September 14

Focus Session: Quantum Computing

Session Code: C4L-H

Location: AV02.17

Time: 14:20 - 15:40

Chair(s): Iuliana Radu; *imec*

14:20 **INVITED: Superconducting Qubit Research at Chalmers**
Jonas Bylander
Chalmers University, Sweden

15:00 **INVITED: A 'Spins Inside' Quantum Processor**
Juan Pablo Dehollain
TU Delft, Netherlands

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