

# ESSCIRC

43<sup>rd</sup> European  
Solid-State Circuits  
Conference

September 11-14, 2017  
Leuven, Belgium

## PROGRAM





September 11-14, 2017  
Leuven, Belgium

# ESSCIRC

43<sup>rd</sup> European  
Solid-State Circuits  
Conference

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Combining a passion for technology with truly inspired engineering, Melexis designs, develops and delivers innovative micro-electronic solutions that enable designers to turn ideas into applications that support the best imaginable future. The company's advanced mixed-signal semiconductor sensor and actuator components address the challenges of integrating sensing, driving and communication into next-generation products and systems that improve safety, raise efficiency, support sustainability and enhance comfort.

A world leader in automotive semiconductor sensors, Melexis has used its core experience in creating chips for vehicle electronics to expand its portfolio of sensors, driver ICs and wireless devices to also meet the needs of smart appliances, home automation, industrial and medical applications. Melexis sensing solutions include magnetic sensors, MEMS sensors (pressure, TPMS, infrared), sensor interface ICs, optoelectronic single point and linear array sensors and Time of Flight. The company's driver IC portfolio incorporates advanced DC & BLDC motor controllers, LED drivers and FET pre-driver ICs, while Melexis has the know-how and expertise to build bridges between components, allowing them to communicate in a clear and fast way, whether wired (e.g. LIN, SENT) or wireless (RKE, RFID).

Melexis is headquartered in Belgium and employs over 1,100 people in 19 locations worldwide. The company is publicly traded on Euronext Brussels (MELE).

For more information, visit [www.melexis.com](http://www.melexis.com)

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On behalf of the entire Organizing Committee, it is our pleasure to welcome you to the 47th European Solid-State Device Research Conference (ESSDERC) and the 43rd European Solid-State Circuits Conference (ESSCIRC) 2017. ESSDERC-ESSCIRC finally returns back to the university town of Leuven, Belgium, many years after having organised a successful ESSDERC-ESSCIRC Conference in 2004 and ESSDERC Conferences in 1999 and 1992, respectively. Since 2003 both ESSDERC and ESSCIRC are running in parallel and have joint keynote speakers and joint focus sessions. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers and system designers. As participant to ESSDERC and ESSCIRC, you not only have the opportunity to become familiar with the latest advances in these fields, but you will meet people who pioneered previous developments, you get access to enhance your international network in micro/nanoelectronics and you will be a witness to previews into emerging fields.

The conference takes place downtown in the city of Leuven, which up to the end of the 13rd century the residence of the Dukes of Brabant. Today Leuven is still the capital of the province of Flemish Brabant. Since 1425 Leuven is the home of KU Leuven, with its ~56000 students the largest university in Belgium. The majority of these students reside in Leuven, and this includes 16% international students. The presence of imec, the largest independent research center in Europe with over 3500 researchers coming from more than 70 different countries, brands Leuven as a world leading hub for micro- and nano-electronics.

This year ESSDERC-ESSCIRC received a total of 393 submissions from 36 countries, of which 241 contributed ESSCIRC and 153 contributed and track invited ESSDERC submissions. About 52% of the submissions came from Europe, 28% from Asia/Pacific and 18% from North America, clearly demonstrating the international character of the conference.

The conference has 4 plenary keynote speakers (Melexis, ON Semiconductor, Analog Devices and Tohoku University), 3 ESSDERC plenary speakers (Intel, SanDisk and RWTH Aachen) and 3 ESSCIRC plenary speakers (Nokia Bell Labs, Ericsson and Columbia University). The selected papers are presented in 43 regular sessions and two focus sessions on Neuromorphic Computing and Quantum Computing, respectively. All this is spread over three days of oral presentations, Tuesday September 12 to Thursday September 14.

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The program also includes an extraordinary social program with a welcome reception and a conference banquet, both with surprise acts. These social events will offer ample opportunities for networking.

In addition, the first day of the event on Monday September 11 will be dedicated to 5 tutorials (1 full-day and 2 half-day tutorials organized by ESSDERC and 2 full-day tutorials organized by ESSCIRC) and to 4 workshops, organized by European and international research and industry consortia. These give extra opportunities for update your knowledge of the state of the art in the covered areas.

We thank the IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) that are the official sponsors of ESSCIRC and ESSDERC, respectively. We also thank all external sponsors that have provided the extra means allowing us to offer the little extras that beyond doubt will make ESSDERC-ESSCIRC 2017 a memorable event in a long tradition.

We are very grateful to the excellent collaboration with the exceptional members of the Organizing Committee and the Technical Program Committee. All members have extremely been devoted and have worked very hard to make ESSDERC-ESSCIRC 2017 yet another successful event. Without their dedication, enthusiasm and professionalism this would not have been possible. We also thank all collaborators and volunteers that helped us out.

Finally, the real success of a conference is based on the support of all the authors who submitted papers to the conference and on the willingness of the keynote, invited, focus session and tutorial speakers to travel to Leuven and to share their knowledge and insights. Their support and efforts are highly appreciated.

Enjoy the 2017 edition of ESSDERC-ESSCIRC and your visit to Leuven, Belgium, and after enjoying and savoring this year's program, we hope to see you all again in Dresden, Germany, for ESSDERC-ESSCIRC 2018.

**Jo De Boeck** and **Georges Gielen**  
Conference General Chairs – ESSDERC-ESSCIRC 2017

**Marc Heyns** and **Guido Groeseneken**  
TPC Chairs – ESSDERC 2017

**Wim Dehaene** and **Patrick Reynaert**  
TPC Chairs – ESSCIRC 2017

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• <b>Patrick Reynaert</b> - KU Leuven, BE	ESSCIRC Workshop Chair

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• <b>Christoph Sandner</b> - Infineon, AT	
• <b>Willy Sansen</b> - KU Leuven, BE	
• <b>Michiel Steyaert</b> - KU Leuven, BE	
• <b>Akira Toriumi</b> - University of Tokyo, JP	

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- **Ru Huang** - Peking University, CN
- **Anil Kottantharayil** - IIT Bombay, IN
- **Maasaki Niwa** - Tohoku University, JP

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## ESSCIRC TECHNICAL PROGRAM COMMITTEE

### Track 8: Analog

- **Peter Mole** - INTERSIL
- **Pieter Harpe** - TU Eindhoven
- Marco Berkhout - NXP
- Stefano D'Amico - University of Salento
- Marcello De Matteis - University of Milano Bicocca
- Gunhan Dündar - Boğaziçi University
- Kimmo Koli - ERICSSON
- Salvatore Pennisi - DIEEI-University of Catania
- Willy Sansen - KU Leuven
- Douglas Smith - Consultant
- Hugo Veenstra - PHILIPS
- Traian Visan - Infineon
- Andreo Vladimirescu - Berkeley University

Track Chair  
Deputy Chair

### Track 9: Data Converters

- **Andrea Baschirotto** - University of Milan-Bicocca
- **Dieter Draxelmayer** - Infineon
- Mario Auer - TU Graz
- Lucien Breems - NXP
- Klaas Bult - Independent Consultant
- Claudius Dan - University POLITEHNICA of Bucharest
- Michael Flynn - University Michigan
- Kofi Makinwa - TU Delft
- Piero Malcovati - University of Pavia
- Franco Maloberti - University of Pavia
- Angelo Nagari - STMicroelectronics
- Maurits Ortmanns - University of Ulm
- Georgi Radulov - TU Eindhoven
- Ana Rusu - KTM
- Jens Sauerbrey - Intel
- Trond Ytterdal - Norwegian University of Science and Technology

Track Chair  
Deputy Chair

### Track 10: RF and mm-wave

- **Domine Leenaerts** - NXP
- **Piet Wambacq** - imec
- Amin Arbabian - Stanford University
- Andreia Cathelin - STMicroelectronics
- Mak Elvis - University of Macau
- Bram Nauta - University of Twente

Track Chair  
Deputy Chair

- Andrea Neviani - University of Padova
- Francois Rivet - University of Bordeaux
- David Ruffieux - CSEM
- Jussi Ryyänen - TU Helsinki
- Kaushik Sengupta - Princeton University
- Lars Sundström - ERICSSON
- Marc Tiebout - Infineon
- Domenico Zito - Aarhus university

### Track 11: Frequency Generation

- **Pietro Andreani** - Lunds University Track Chair
- **Andrea Bevilacqua** - University of Padova Deputy Chair
- Jaehyouk Choi - Ulsan National University (UNIST)
- Martin Flatscher - Infineon
- Peter Kennedy - University College Cork
- Antonio Liscidini - University of Toronto
- Baudouin Martineau - CEA
- Kenichi Okada - Tokyo Institute of Technology
- Carlo Samori - Politecnico di Milano
- Alexandre Siligaris - CEA
- Bogdan Staszewski - UC Dublin
- Francesco Svelto - University of Pavia

### Track 12: Wireless and wireline systems

- **Sven Mattisson** - ERICSSON Track Chair
- **Jan Craninckx** - imec Deputy Chair
- Jean Baptiste Begueret - University of Bordeaux
- Didier Belot - CEA-LETI
- Marc Borremans - Huawei
- Giuseppe Gramegna - Huawei
- Qiuting Huang - ETH Zürich
- Andrea Mazzanti - University of Pavia
- Dominique Morche - CEA
- Takashi Oshima - HITACHI
- Yorgos Palaskas - Intel
- Silvian Spiridon - Broadcom
- Filip Tavernier - KU Leuven
- Thomas Toifl - IBM
- Dixian Zhao - SouthEast University
- Josef Zipper - Panthronics AG

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### Track 13: Sensors, imagers and biomedical

- **Angel Rodriguez-Vazquez** - CSIC Track Chair
- **Andreas Demosthenous** - London's Global University Deputy Chair
- Ralf Brederlow - Texas Instruments
- Werner Brockherde - Fraunhofer IMS
- Eugenio Cantatore - TU Eindhoven
- Antoine Dupret - CEA
- Christian Enz - EPFL
- Robert Henderson - The University of Edinburgh
- Michael Mark - Infineon
- Matteo Perenzoni - FBK
- Albrecht Roethermel - University of Ulm
- Chris (Jacques) Rudell - University of Washington
- Hanspeter Schmid - FH Nordwestschweiz
- Roland Thewes - TU Berlin

### Track 14: Digital, security and memory

- **Stefan Rusu** - TSMC Track Chair
- **Tobias Gemmeke** - imec Deputy Chair
- Atila Alvandpour - Linköping University
- Andreas Burg - EPFL
- Sylvain Clerc - STMicroelectronics
- Shidhartha Das - ARM
- Tobias Noll - RWTH Aachen
- Viktor Öwall - Lunds University
- Praveen Raghavan - imec
- Christoph Studer - Cornell University
- Hannu Tenhunen - KTH
- Ramses Valvekens - Easics
- Ingrid Verbauwhede - KU Leuven

### Track 15: Power management

- **Michiel Steyaert** - KU Leuven Track Chair
- **Christoph Sandner** - Infineon Deputy Chair
- Ke-Horng Chen - NCTU Taiwan
- Johan Janssens - ON Semiconductor
- Ravi Karadi - NXP
- Lauri Koskinen - University of Turku
- Yiannos Manoli - University of Freiburg
- Bill Redman-White - University of Southampton
- Drago Strle - Uni Ljubljana
- Toru Tanzawa - Shizuoka University
- Bernhard Wicht - Leibniz University Hannover



## WELCOME TO LEUVEN

With about 100.000 inhabitants, Leuven is well known as a university city. It is the home of the biggest university in Belgium, with more than 40.000 students. Founded in 1425 by Papal Bull under Martinus V, it is also the oldest university in Belgium.

The city of Leuven itself came in full bloom a few centuries earlier. Up to the end of the 13rd century, it was the residence of the Dukes of Brabant. Town and university have known many periods of prosperity. The town hall, churches, cloisters and colleges stand silent witness of those days and make Leuven an interesting place, rich in historical buildings that radiate a magic of their own. Major tourist attractions are the more than 550 year old town hall, the Great Beguinage, the University Library, the St. Peters Cathedral and the Papal college.

Triggered by the presence of imec, the largest independent research center in Europe with over 3500 researchers coming from more than 70 different countries, Leuven became a world leading center for micro and nano-electronics. KU Leuven and imec have created almost 200 spin-off companies. Leuven is also hosting the headquarters of AB INBEV, the largest brewery in the world.

Leuven is only 20 km away from Brussels, the capital of Belgium and hearth of Europe. It is ideally situated to visit world famous places like Antwerp, Gent and Bruges. Even the seaside or the Ardennes are less than 2 hours away.

The venue of the conference events, including workshops and tutorials, will be in the center of Leuven.

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## GETTING AROUND LEUVEN

### By Bus

The main local bus terminal is located next to the railway station (if you leave the station, it is on your right hand side). The busses easily reach Leuven centre and surrounding areas. Local busses are run by De Lijn ([www.delijn.be](http://www.delijn.be))

### By Bike

You can hire bikes at a number of different locations in Leuven. ([www.visitleuven.be/en/bike](http://www.visitleuven.be/en/bike))

### By Taxi

Taxis can be found at the Leuven train station (in front of the main building) and at Smoldersplein (near the courthouse).

Taxi companies in Leuven:

- Taxi Alex  
Bierbeekstraat 116, 3001 Leuven (Heverlee),  
Tel. +32 16 29 16 16
- Taxi's Jenny NV  
Diestsesteenweg 489, 3010 Leuven (Kessel-Lo),  
Tel. +32 16 25 35 65
- Taxi Gerard  
Wipstraat 27, 3010 Leuven (Kessel-Lo),  
Tel. +32 16 25 09 99
- Cordons-Van Minsel BVBA  
Hoveniersdreef 31, 3001 Leuven (Heverlee),  
Tel. +32 16 22 20 00



## KU LEUVEN CAMPUS OF SOCIAL SCIENCES

The ESSCIRC/ESSDERC Conference takes place in the city center of Leuven, at the:

**KU LEUVEN Campus of Social Sciences  
Parkstraat 45, 3000 Leuven, Belgium**

## HOW TO REACH THE VENUE

From the train station

### By Foot

The Faculty of social Sciences is situated at walking distance (about 15 minutes) from the station. Follow 'Maria-theresiastraat' until it changes into 'Andreas Vesaliusstraat'. Then follow the 'Andreas Vesaliusstraat' up to the crossing with the 'Parkstraat'. Turn right here.

You will find the campus about 100m further at your right side.

### By bus

Take the bus with number 4, 5 or 6 and alight at the stop called 'Remy' in the 'Andreas Vesaliusstraat'. Follow the 'Andreas Vesaliusstraat' until it crosses with the 'Parkstraat'. Then turn right. You will find the campus about 100m further at your right side.

## SESSIONS

Sessions will be located in different buildings inside and just outside the Campus:

- **JOINT PLENARY SESSIONS**

VESALIUS AULA (Andreas Vesaliusstraat, 3000 Leuven), just outside the Campus. The Andreas-Vesalius street is the continuation of the Maria-Theresiastreet and connects the campus directly to the train station.

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- **ESSCIRC SESSIONS**

Room **AP 00.15** Auditorium Max Weber (**AP**)  
(Parkstraat 51, 3000 Leuven) inside the Campus  
Room **AV 91.12** Auditoria complex (**AV**)  
(Parkstraat 49, 3000 Leuven) inside the Campus  
Room **AV 01.12** Auditoria complex (**AV**)  
(Parkstraat 49, 3000 Leuven) inside the Campus  
Room **AV 03.12** Auditoria complex (**AV**)  
(Parkstraat 49, 3000 Leuven) inside the Campus

- **ESSDERC SESSIONS**

Room **AP 01.30** Auditorium Jean Monnet (**AP**)  
(Parkstraat 51, 3000 Leuven), same building as Max Weber  
Auditorium but upstairs, inside the Campus  
Room **AV 00.17** Auditoria complex (**AV**)  
(Parkstraat 49, 3000 Leuven) inside the Campus  
Room **AV 02.17** Auditoria complex (**AV**)  
(Parkstraat 49, 3000 Leuven) inside the Campus

- **TUTORIALS** (Monday 11 September)

Room **AV 01.12** Integrated Power Management in Research  
and Industry  
Room **AV 03.12** The Hidden Challenges of 5g  
Room **AV 00.17** Beyond Cmos  
Room **AV 02.17** Sensors for the IoT Era  
Room **AV 02.17** Neuromorphic Computing with Emerging  
Synaptic Devices

- **WORKSHOPS** (Monday 11 September)

Room **AV 04.17** Connect  
Room **AV 91.12** Mos-AK  
Room **AP 00.15** Sinano - Nereid  
Room **AP 01.30** Semiconductor Memories

- **WOMEN IN CIRCUITS** (Tuesday at 12:30 pm)

At FlexiSpace inside KU Leuven Agora Learning Centre  
(E. Van Evenstraat 4 - B-3000 Leuven) in the KU LEUVEN  
Campus of Social Sciences

- **ELECTRONIAD QUIZ** (Tuesday at 7:00 pm)

Alma 2 - E. Van Evenstraat 2, Leuven

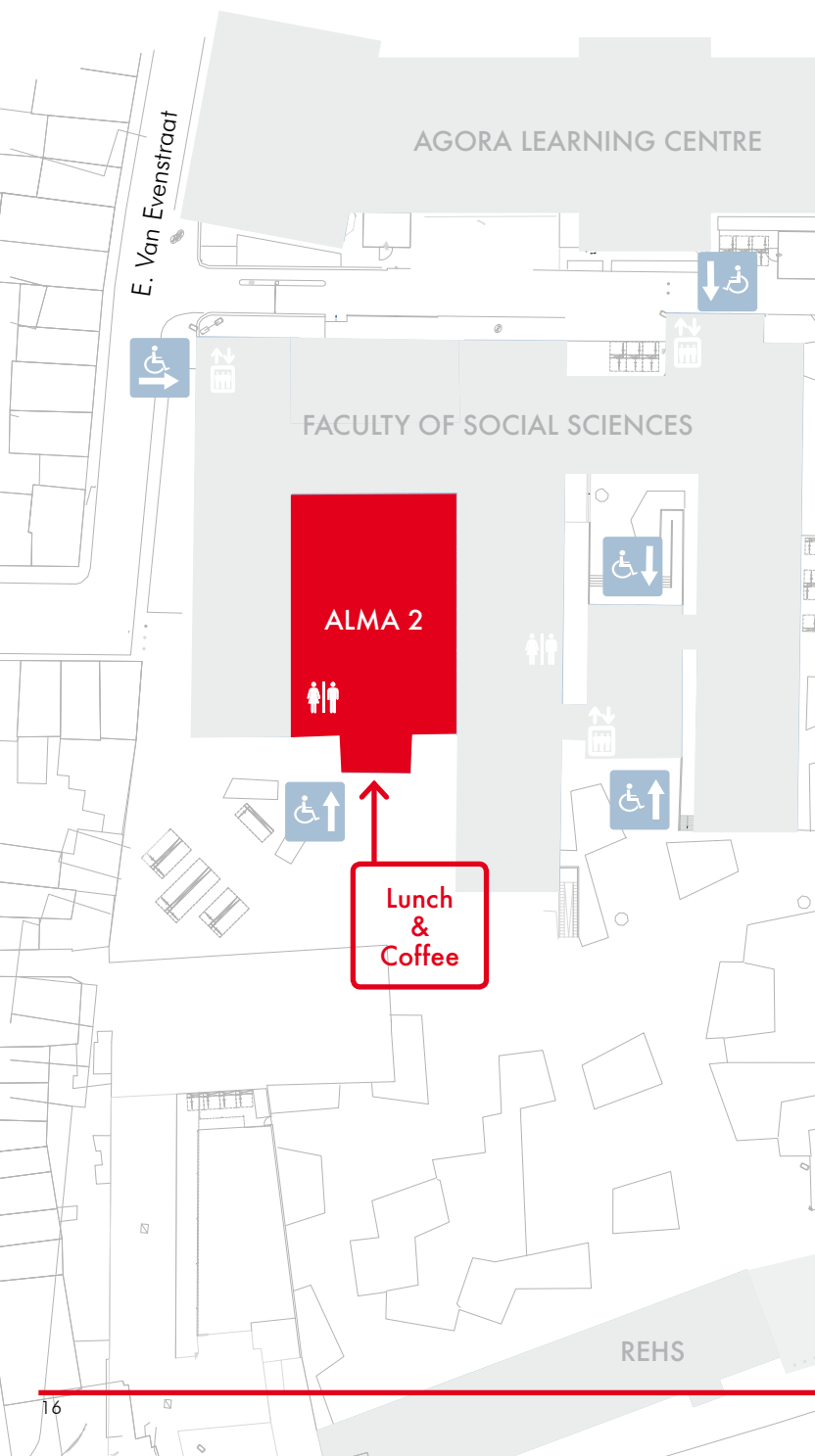
- **REGISTRATION DESK**

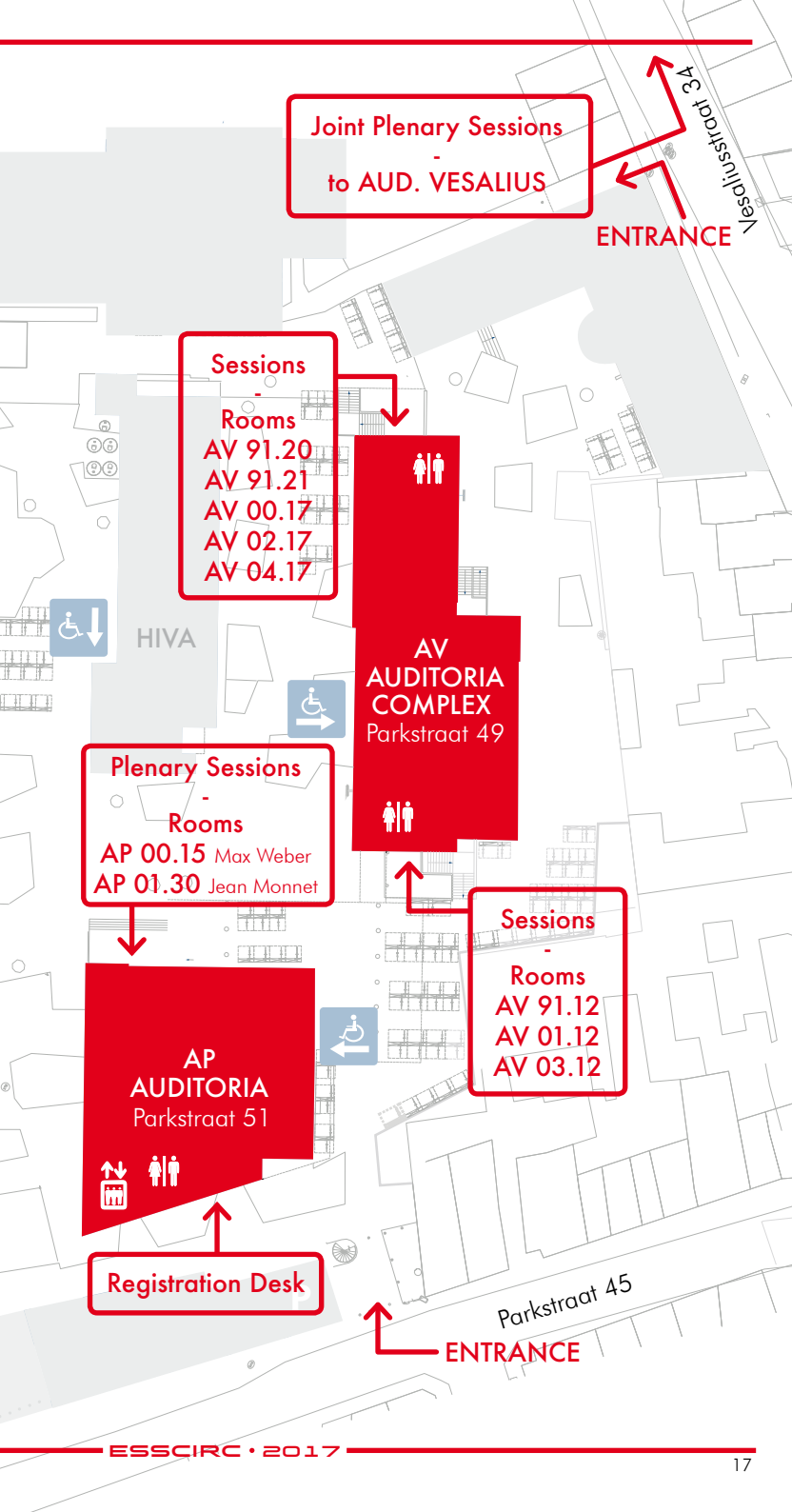
The Registration Desk will be located in the Max Weber/  
Jean Monnet building (AP Auditoria).

**Registration Desk will move to VESALIUS AULA only  
on Tuesday from 8.00 till 10.00 am.**

- **COFFEE BREAKS AND LUNCHES**

Breaks will be held in the Student Restaurant Alma 2  
(Parkstraat 45, inside the Campus), which will be closed for  
the public during the conference.





Joint Plenary Sessions  
to AUD. VESALIUS

ENTRANCE

Vesaliusstraat 34

Sessions

Rooms

AV 91.20  
AV 91.21  
AV 00.17  
AV 02.17  
AV 04.17



AV  
AUDITORIA  
COMPLEX  
Parkstraat 49



Plenary Sessions

Rooms

AP 00.15 Max Weber  
AP 01.30 Jean Monnet

AP  
AUDITORIA  
Parkstraat 51



Registration Desk

Sessions

Rooms

AV 91.12  
AV 01.12  
AV 03.12

Parkstraat 45  
ENTRANCE

# Morning Tutorials - Monday September 11th, 2017

Time	AV01.12	AV03.12	AV00.17	AV02.17
	<b>ESSCIRC Tutorials</b>		<b>ESSDERC Tutorials</b>	
08:00-08:30	Integrated Power Management in Research and Industry	The Hidden Challenges of 5G	Beyond CMOS	Sensors for the IoT Era
08:30-09:00	Registrations	Registrations	Registrations	Registrations
09:00-10:00	Integrated Switched-capacitor Power Converters: a Feasible Way to Get High Efficiency Power Conversion in Standard CMOS Technology <i>Gerard Villar Piqué</i>	What is Required of 5G to Make It Attractive for MTC? <i>Yao-Hong Liu</i>	Introduction to Beyond CMOS <i>Iuliana P. Radu</i>	Smart Sensors for Environmental Monitoring <i>Florin Udrea</i>
10:00-10:30	Coffee Break			
10:30-11:30	Integrated Inductive and Hybrid DC-DC Converters <i>Giovanni Frattini</i>	Programmable mm-Wave Transmitters: Generalized PA Architectures for Frequency and Back-off Reconfigurability <i>Kaushik Sengupta</i>	Tunnel FETs – Status and Prospects <i>Nadine Collaert</i>	Sensors for Health Monitoring <i>Patrick Mercier</i>
11:30-12:30	Making Magnetics Disappear - Integrated Magnetics for Power Management <i>Cian O'Mathuna</i>	Implementing Massive MIMO Systems: Coarse Processing Gives Fine Performance <i>Liesbet Van der Perre</i>	Negative Capacitance FETs: Physics, Materials and Devices <i>Asif Islam Khan</i>	Sensors for Automotive Industry <i>Appo van der Wiel</i>
12:30-13:30	Lunch			

Afternoon Tutorials - Monday September 11th, 2017				
Time	AV01.12	AV03.12	AV00.17	AV02.17
	<b>ESSCIRC Tutorials</b>		<b>ESSDERC Tutorials</b>	
12:30-13:30	Integrated Power Management in Research and Industry	The Hidden Challenges of 5G	Beyond CMOS	Neuromorphic Computing with Emerging Synaptic Devices
13:30-14:00	Lunch		Lunch	
14:00-15:00	Vibrational Harvesters for Wireless Sensing Applications <i>Stefano Stanzione</i>	Integrated Wide-band Baseband Filters and Narrow-band RF Filters for 5G <i>Bram Nauta</i>	Towards Functionality-Enhanced Devices: Controlling the Modes of Operations in Three-Independent-Gate Transistors <i>Pierre-Emmanuel Gaillardon</i>	Analog Synapse Devices based on Interface Resistive Switching for Neuromorphic Systems <i>Hyunsang Hwang</i>
15:00-15:30	Coffee Break			
15:30-16:30	Power Management Design for Highly Integrated Automotive ICs <i>Bernhard Wicht</i>	Challenges in 5G Transmitter Design <i>Christian Fager</i>	Spintronics in the Context of Computation <i>Titash Rakshit</i>	Emerging Memories for Neurocomputing <i>Dmitri Strukov</i>
16:30-17:30	1 kV On-chip, Hard to Resist? <i>Valentijn De Smedt</i>	Opto Implementation Challenges for 5G Networks <i>Francesco Testa</i>	Introduction to Quantum Computing <i>Ronald Hanson</i>	Accelerating Backpropagation Training with Non-Volatile Memory: Devices, Circuits and Architecture <i>Geoffrey Burr</i>

Workshops - Monday September 11, 2017				
AV 04.17	AV 91.12	AP 00.15	AP 01.30	
08:00 Registrations	08:00 Registrations	08:00 Registrations		
08:30 - 10:10 CONNECT <i>Aida Todri-Sanial</i> <i>Salvatore M. Amoroso</i> <i>Benjamin Uhlig</i> <i>Gage Krieger Hills</i> <i>Esko Kauppinen</i>	08:30 - 10:10 MOS-AK <i>Jim Greer</i> <i>Marcelo Pavanello</i>	09:00 - 10:45 SINANO - NEREID <i>Enrico Sangiorgi</i> <i>Francis Balestra</i> <i>Francisco Ibanez</i> <i>Jouni Ahopelto</i> <i>Clivia Sotomayor Torres</i>	08:30 - 11:15 SEMICONDUCTOR MEMORIES <i>Francisco Gamiz</i> <i>Kilho Lee</i> <i>Manfred Horstman</i> <i>Elisa Vianello</i>	
Coffee 10:10 - 10:40	Coffee 10:10 - 10:30	Coffee 10:45 - 11:00	Coffee 11:15 - 11:45	
10:40 - 12:30 CONNECT (Continued) <i>Jean Dijon</i> <i>Benjamin Uhlig</i> <i>Marleen van der Veen</i>	10:30 - 12:30 MOS-AK <i>Wim Schoenmaker</i> <i>Jean-Pierre Raskin</i> <i>Chika Tanaka</i>	11:00 - 12:45 SINANO - NEREID (Continued) <i>Anda Mocuta</i> <i>Yann Deval</i> <i>Montserrat Fernandez-Bolanos</i> <i>Steve Stoffels</i> <i>Stéphane Monfray</i>	11:45 - 13:15 SEMICONDUCTOR MEMORIES (Continued) <i>Pierre Fazan</i> <i>Guohua Hu</i>	
Lunch 12:30 - 14:00	Lunch 12:30 - 14:00	Lunch 12:45 - 14:00	Lunch 13:15 - 14:30	
14:00 - 15:10 CONNECT (Continued) <i>Shu-Jen Han</i> <i>Bingan Chen</i>	14:00 - 15:00 MOS-AK (Continued) <i>Nicolas Cordero</i> <i>Ashkhen Yesayan</i>	14:00 - 16:00 SINANO - NEREID (Continued) <i>Danilo Demarchi</i> <i>Holger Schmid</i> <i>Georgios Fagas</i> <i>Thanasis Dimoulas</i> <i>Enrico Sangiorgi</i>	14:30 - 16:00 SEMICONDUCTOR MEMORIES (Continued) <i>Philippe Galy</i> <i>Sorin Cristoloveanu</i> <i>Joris Lacord</i>	
Coffee 15:10 - 15:40	Coffee 15:00 - 15:30		Coffee 16:00 - 16:30	
15:40 - 17:00 CONNECT (Continued) <i>Bernd Gotsmann</i> <i>Aida Todri-Sanial</i>	15:30 - 17:00 MOS-AK (Continued) <i>Denis Flandre</i> <i>Benjamin Iniguez</i> <i>Saravana Maruthamuthu</i>		16:30 - 17:45 SEMICONDUCTOR MEMORIES (Continued) <i>Asen Asenov</i> <i>Andy Pickering</i>	

# Tuesday September 12th, 2017

Time	AP00.15	AV91.12	AV01.12	AV03.12	AP01.30	AV00.17	AV02.17
08:00-08:30	Vesalius -- Registrations						
08:30-09:00	Vesalius -- Conference Opening & Welcome (presentation by SSC society and EDS society)						
09:00-09:40	Vesalius -- A1L-A: ESSDERC/ESSCIRC Joint Plenary 1: Françoise Chombar, Melexis Engineering a Safe, Clean & Comfortable Future						
09:40-10:20	Vesalius -- A2L-A: ESSDERC/ESSCIRC Joint Plenary 2: Peter Real, Analog Devices Navigating without a Moore's Law Compass						
10:20-11:00	Coffee Break						
11:00-12:20	A3L-B References	A3L-C RF Receivers and Detectors	A3L-D Digital Accelerators	A3L-E Optical Sensors	A3L-F Resistive RAM	A3L-G Cross-Domain Compact Modelling	A3L-H Focus Session: Beyond CMOS Devices I
12:20-14:00	Lunch						
14:00-15:20	A4L-B Amplifiers and Comparators	A4L-C Oscillators	A4L-D Wireline and Optical		A4L-F Alternative Device Simulations	A4L-G Parameter Extraction	A4L-H Focus Session: Beyond CMOS Devices II
15:20-15:50	Coffee Break						
15:50-16:30	Room: AP00.15 A5L-B, ESSCIRC Keynote 1: Yves Baeyens: Solving Capacity Bottlenecks in Fixed Access Comms				Room: AP01.30 A5L-F, ESSDERC Keynote 1: Ian Young: Principles and Trends in Quantum Nano-Electronics & Nano-Magnetics for Beyond-CMOS Computing		
16:40-18:00	A6L-B Energy Harvesting	A6L-C Advanced ADC Techniques	A6L-D Digital-intensive Frequency Synthesis	A6L-E Digital Processors		A6L-G Modelling of Emerging Devices	A6L-H 2D Material Devices
18:00-19:00	ESSCIRC TPC Mtg.	ESSDERC TPC Mtg.					
19:00-21:00	ESSDERC/ESSCIRC 2017 Welcome Reception: Jubilee Hall						

Legend

CIRC = ■

CIRC Keynote = ■

DERC = ■

DERC Keynote = ■

Joint = ■

## Wednesday September 13th, 2017

Time	AP00.15	AV91.12	AV01.12	AV03.12	AP01.30	AV00.17	AV02.17
08:30-08:45							
08:45-09:25							
09:25-10:10							
10:10-12:10	B2L-B High Speed ADC	B2L-C Transmitters and Power Amplifiers for mm-Wave and IoT	B2L-D Biomedical Circuits and Systems		B2L-F Widebandgap Power Devices	B2L-G Advanced CMOS Characterization and Reliability	B2L-H Emerging Memory Technologies
12:10-13:30							
13:30-14:10							
14:20-15:40	B4L-B High Efficiency ADC	B4L-C 5G and mm-Wave Frequency Synthesis	B4L-D Machine Learning and Neuromorphic Computing	B4L-E Linear Regulators	B4L-F FinFet and Nanowire Simulations	B4L-G Traps and Noise	B4L-H 2D Material Integration
15:40-16:00							
18:00-23:00							
Legend	CIRC = <span style="color: red;">■</span>	CIRC Keynote = <span style="color: red;">■</span>	DERC = <span style="color: blue;">■</span>	DERC Keynote = <span style="color: blue;">■</span>	Joint = <span style="color: green;">■</span>		

# Thursday September 14th, 2017

Time	AP00.15	AV91.12	AV01.12	AV03.12	AP01.30	AV00.17	AV02.17
08:30-09:00				Vesalius -- Awards Ceremony			
09:00-09:40				Vesalius -- C1L-A: Joint Plenary 4: Tetsuo Endoh, Tohoku University Spintronics Applications: STT-MRAM & Non Volatile Logic			
09:40-10:20				Coffee Break			
10:20-12:00	C2L-B Power Management and Harvesting	C2L-C Embedded Memories	C2L-D Wireless SOC	C2L-E Focus Session: Neuromorphic Computing	C2L-F Photonics / Microwave / Harsh Environment	C2L-G Advanced CMOS Technology	C2L-H Microfluidics and TFTs
12:00-13:30				Lunch			
13:30-14:10	Room AP00.15 C3L-B, ESSCIRC Keynote 3: Harish Krishnaswamy, Columbia Univ. - Integrated Antenna-Interface Components				Room AP01.30 C3L-F, ESSDERC Keynote 3: David DiVincenzo - Control Systems for Quantum Computers		
14:20-15:40	C4L-B DC-DC Converters	C4L-C Sensor Interfaces	C4L-D Low Power Radios		C4L-F Modelling and Measurement of Alternative Material Devices	C4L-G High Mobility Materials and Nanowires	C4L-H Focus Session: Quantum Computing
19:00	ELECTRONIAD Quiz -- Celebrating Easics 25th Anniversary						

Legend

CIRC = ■

CIRC Keynote = ■

DERC = ■

DERC Keynote = ■

Joint = ■

## LANGUAGE

The official language of the conference is English: no simultaneous translation will be available.

## REGISTRATION DESK

The Registration Desk will be located in the Max Weber/Jean Monnet building (AP Auditoria) and it will be open the following hours throughout the Conference:

- Monday 11 September: 8.00 am - 6.00 pm
- Tuesday 12 September: 8.00 am - 5.00 pm
- Wednesday 13 September: 8.00 am - 4.00 pm
- Thursday September: 9.00 am - 4.00 pm

**Registration Desk will move to VESALIUS AULA only on Tuesday from 8.00 till 10.00 am.**

## BADGES

Badges must always be visibly worn during sessions, coffee breaks and lunches, and also during social program activities.

## COFFEE BREAKS AND LUNCHES

Coffee breaks and lunches will be served to registered participants wearing their badges. Accompanying persons have no access to scientific sessions nor to coffee breaks and lunches. Please note that vegetarian dishes will be on daily menu; for other special needs, we will try to serve a good variety of food so that it will be easier for you to get some alternatives in case of special diet restrictions.

## PERSONS WITH SPECIAL NEEDS

Every effort has been made to ensure that people with special needs are catered for during the conference. Should you require any specific assistance, please let us know in advance to enable to assist in making your stay at the conference a pleasant and comfortable one.

## INTERNET / WI-FI

Wi-Fi connection will be available on site.

## CERTIFICATE OF ATTENDANCE

Certificates will be sent by email upon request to [essxxrc@sistemacongressi.com](mailto:essxxrc@sistemacongressi.com), after the Conference.

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## **LIABILITY**

In registering for the conference, participants agree that neither the Scientific/Organizing Committees nor the Organizing Secretariat assumes any liability.

## **CURRENCY**

The local currency is € (Euro). Automatic teller machines and exchange offices are available in Leuven city centre. Most hotels, restaurants and shops accept major credit cards but please always check first!

## **ELECTRICITY**

Electricity is 220-230V, 50 Hz. Belgian plugs have two round pins.

## **CALLING CODES**

Belgium country code : +32 (or 00 32)

Leuven: +32 (0)16

## **EMERGENCY NUMBERS**

European emergency number: 112

## **PHARMACY APOPARK**

Address: Tiensestraat 81, 3000 Leuven

Phone: 016/22.20.48 Website

Opening hours: Mo - Fr: 8.30 am - 18.00 pm, Sa 8.30 am to noon.

## **STORE OPENING HOURS**

Most shops are open from Monday till Saturday, 10:00 am - 18:00 pm

## **SMOKING**

No smoking in public places (e.g. airports, train stations, schools, universities, restaurants, bars and cafes, government buildings) and on public transport.



## WELCOME COCKTAIL AT JUBILEE HALL

**Tuesday 12 September**

From 7 pm until 9 pm

It is located in the University Hall, the university's main building in the city centre.

### University Hall, Naamsestraat 22, Leuven

This prestigious building of 1317 was originally the municipal Cloth Hall and only comprised a ground floor in Gothic style. In 1432 the newly founded university was housed in the wing on the Krakenstraat. The hall was used as a lecture hall until the First World War. In 1679 the city sold the entire building to the University that immediately built the baroque first floor. In 1723 the Rega wing was added (classical sandstone façade overlooking Oude Markt).

### Rate

Free for conference participant

Additional Welcome Cocktail ticket: € 30,00



## **GALA DINNER AT AUTOWORLD**

**Wednesday 13 September**

From 6 pm until 11.30 pm

**Jubelpark 11, 1000 Brussels**

The museum's housing treasures of the history of the motor car, thanks to Ghislain Mahy's and his family's gamble, and the gentle but uncontested force of persuasion of a prince who later became King Albert II. They were helped by the combined support of the ministerial responsibilities of the late vice-president of Autoworld, Minister Louis Olivier, formerly in charge of public works, and President Herman De Croo, communications minister for eight years. Autoworld is a highly-colorful environment adapted for teaching purposes and created to continue evolving on a non-stop basis.

Decades of evolution in technology, comfort, safety and increasing concern with the environment are on display here via superb coaches and countless motorized vehicles. From the earliest models of the distant past to contemporary cars that prefigure the automobile of tomorrow and beyond, the visitor is guided through the fabulous history of the motor car thanks to technical but easily comprehensible commentaries.

### **Rate**

Free for conference participant

Additional Gala Dinner ticket: € 150,00

### **How to get**

Buses will be provided from Leuven to Autoworld and back (no intermediate stops will be possible). Information will be available at the registration desk.

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

### **ESSCIRC 2017 Tracks**

- Analog
- Data Converters
- RF and mm-Wave
- Frequency Generation
- Wireless and Wireline Systems
- Sensors, Imager and Biomedical
- Digital, Security and Memory
- Power Management

### **ESSCIRC/ESSDERC Focus Tracks**

- Neuromorphic Computing
- Quantum Computing

## FRANÇOISE CHOMBAR

CEO Melexis, Belgium

**Engineering a safe, clean and comfortable future**



Ms. Françoise Chombar has been the Chief Executive Officer of Melexis NV, since 2004 and has been its Managing Director since February 15, 2011. Ms. Chombar serves as the Chief Executive Officer of Melexis Microelectronic Integrated Systems N.V. She is the Co-Founder of Melexis. Ms. Chombar served as Chief Operating Officer of Melexis NV since 1994. She served as Chief Executive Officer for Operations, Sales and Human Resources of Epiq Nv since 2004 and its Acting Chief Operating Officer since 1994. She served as Planning Manager at Elmos GmbH, a German semiconductor company, from 1986 to 1989 and as Commercial Assistant at Michel Vande Wiele n.v., a Belgian textile equipment manufacturer, from 1984 to 1985. Since 1989 she served as a Operations Manager of Elex-Xtrion group since 1989. Ms. Chombar has been a Director of Epiq NV since 1996 and Melexis NV since 1996. She has been an Independent Non-Executive Director of Umicore S.A. since April 26, 2016. She served as an Independent Director of EVS Broadcast Equipment S.A. since May 2012. She served as a Director of Elex-Xtrion group. She's been mentor of the Women's network Sofia since 2000, a member of Women on Board since 2011 and honorary ambassador of the Department of Applied Languages of the University of Gent since January 2012.

Ms. Chombar holds a Master Degree as Interpreter in Dutch, English and Spanish from the University of Gent.

## TETSUO ENDOH

Professor Tohoku University, Japan

### Spintronics applications: STT-MRAM and Non Volatile Logic



Tetsuo Endoh joined ULSI Research Center Toshiba Co. in 1987 and was engaged in the R&D of NAND Memory. He became a lecturer at the Research Institute of Electrical Communication, Tohoku University in 1995. He is a professor at the Department of Electrical Engineering, the Graduate School of Engineering, Tohoku University and director of the Center for Innovative Integrated Electronic Systems (CIES). His current interests are novel 3D structured device technology, such as Vertical MOSFETs; high-density memory, such as SRAM, DRAM, 3D-NAND memory and STT-MRAM; and beyond-CMOS technology, such as spintronics-based non-volatile Logic for ultralow power systems such as mobile systems, AI systems and IoT systems.

He is also interested in power-management technology, such as GaN on Si based power devices and power integrated circuits with low energy loss and low power consumption for automotive applications. He received the 14th Prime Minister's Award for its Contribution to Industry-Academia-Government Collaboration in 2016. He received 2017 National Invention Award "the 21st century Encouragement of Invention Prize" on June 12th.

**PETER REAL**

Senior VP & CTO Analog Devices Inc.

**Navigating without a Moore's Law Compass**



Peter Real is Senior Vice President and Chief Technology Officer of Analog Devices. In this role, Mr. Real works closely with ADI's business units and manufacturing operations to provide a long term technology and capability vision for the company which drives ADI's competitive advantage. He is responsible for the identification, sourcing, and nurturing of new business, technology, and research opportunities while also being responsible for the development of foundation capabilities in support of current and future needs. Previously, Mr. Real held the positions of Vice President of the High Speed Products and Technology Group, Vice President of the Linear and Radio Frequency Products and Technology Group, Vice President of the Radio Frequency and Networking Products Group, and various design engineering and product line leadership roles.

Mr. Real holds Bachelor of Science and Master of Science degrees in Electrical Engineering, and is the author or co-author of nine patents.

## HANS STORK

Senior VP & CTO ON Semiconductor, USA

### Smart Power for Automotives



Dr. Hans Stork is Senior Vice President and Chief Technology Officer (CTO) at ON Semiconductor. He oversees the development of wafer process technologies, modeling and design kits, design libraries, as well as packaging technologies and assembly support.

Prior to joining ON Semiconductor, Dr. Stork was Group Vice President and CTO of the Silicon Systems Group at Applied Materials. From 2001 to 2007 he was Senior Vice President and the CTO of Texas Instruments. Before that, Dr. Stork held various R&D and management positions at Hewlett Packard Laboratories and at IBM's T.J. Watson Research Center.

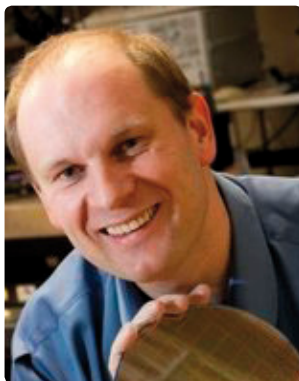
Dr. Stork serves on the supervisory board of ASML, is a member of the Scientific Advisory board at imec, and has previously served on the boards of Sematech and the SRC. He is also a longstanding member of the SIA Technology Strategy Committee. He authored more than 100 cited papers and holds 11 U.S. patents. He was elected IEEE Fellow in 1994, and served on several IEEE sponsored conference program committees, and is currently vice-chair of the Technical Field Awards Council and a member of the Awards Policy and Portfolio Review Committee.

Dr. Stork was born in Soest, The Netherlands, and received the Ingenieur degree in electrical engineering (EE) from Delft University of Technology, Delft, The Netherlands, and holds a PhD in EE from Stanford University.

**YVES BAEYENS**

Nokia Bell labs, Belgium

**Solving Capacity Bottlenecks in Fixed Access Comms**



Yves Baeyens received the PhD degree in Electrical Engineering from the KU Leuven, Belgium in 1997. After his PhD, he spent one and a half year as a visiting scientist at the Fraunhofer Institute for Applied Solid-State Physics in Freiburg, Germany.

Since 1998, he has been with Bell Laboratories, currently the research division of Alcatel-Lucent. He is now Director of the High-Speed Electronics and Opto-Electronics Research Department in Murray Hill, NJ. His main research interests are the architecture, the design and technology of electronics and opto-electronic circuits for terabit optical and multi-gigabit wireless applications.

Yves Baeyens is a Fellow of IEEE and was nominated and selected for the National Academy of Engineering 2009 US and 2011 US/EU Frontiers in Engineering Symposia. He authored or co-authored over 100 publications on high-speed semiconductor technologies and circuits.

Since 2003, Yves Baeyens is an adjunct professor at the Department of Electrical Engineering of Columbia University, New York City, NY, where he teaches a graduate course on advance microwave circuit design.

**HARISH KRISHNASWAMY**

Professor Columbia University, USA

**Integrated Antenna-Interface Components –  
A Blessing for Wireless Transceivers**



Harish Krishnaswamy received the B.Tech. degree in Electrical Engineering from the Indian Institute of Technology-Madras, India, in 2001, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Southern California (USC) in 2003 and 2009, respectively. He joined the EE department of Columbia University as an Assistant Professor in 2009.

He received the IEEE International Solid State Circuits Conference (ISSCC) Lewis Winner Award for Outstanding Paper in 2007. He also received the Best Thesis in Experimental Research Award from the USC Viterbi School of Engineering in 2009, and the DARPA Young Faculty Award in 2011.

## SVEN MATTISSON

Corp. Senior Expert Ericsson, Sweden

### Overview of 5G requirements and future wireless networks



Sven Mattisson received his PhD in Applied Micro Electronics from Lund University in 1986. From 1987 through 1994 he was an associate professor in Applied Micro Electronics in Lund where his research was focused on circuit simulation and analog ASIC design. In 1995 he joined Ericsson in Lund to work on cellular handset development.

Presently he is with Ericsson Research in Lund, where he holds a position as senior expert in analog system design. Since 1996 he is also an adjunct professor at Lund University. Dr. Mattisson is a coinventor of Bluetooth and has been serving as technical program committee member for the International Solid-State Circuits Conference and the European Solid-State Circuits Conference. Presently he is working on 5G radio circuits

All tutorials will be held on Monday 11 September.  
08.00 - 09.00 Registrations

## INTEGRATED POWER MANAGEMENT IN RESEARCH AND INDUSTRY

Tutorial Organizer: Gerard Villar Piqué, NXP Semiconductors

Room **AV 01.12**

**GERARD VILLAR PIQUÉ**

09.00 - 10.00

**Integrated switched-capacitor power converters:  
a feasible way to get high efficiency power conversion  
in standard CMOS technology**

### Abstract

Since they do not require inductors, switched-capacitor power converters (SCPC) have become a feasible way to implement more efficient power converters/voltage regulators fully integrated in standard CMOS technologies. This has increased the interest for them in both industry and academia. However, their performance is strongly impacted by the non-idealities of the integrated components, making their design challenging. Also, providing an efficient voltage regulation for a wide range of input voltage is not straightforward. This tutorial will cover the most relevant design aspects, including different tricks to overcome the main sources of energy loss, different implementations for the floating capacitors, the most popular control methods and topologies comparison. Different examples from industry and academy will be provided.

### Bio

Gerard Villar Piqué received the M.Sc. degree in 2001, and the Ph.D. degree in 2007 from the Technical University of Catalonia, Barcelona. In April 2008, he joined the Mixed-Signal Circuits and Systems Group, at the Research Department of NXP Semiconductors, Eindhoven (The Netherlands). As Principal Scientist of the Power Management team at AMSIP, he is involved in research on integrated power management systems. His main research areas include mixed-signal and analog microelectronics design, as well as power management systems (including switched-mode power supplies), with special focus in low-power fully-integrated switched-capacitor DC-DC converters. He has published a book on monolithic integration of inductive switching power converters. He is a member of the Technical Program Committee of ESSCIRC, ISSCC and PowerSoC.

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## COFFEE BREAK

10.00 - 10.30

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## GIOVANNI FRATTINI

10.30 - 11.30

### Integrated inductive and hybrid DC-DC converters

#### Abstract

Starting from the basic principles of switching power converters, this tutorial will discuss the techniques associated with design of these kind of devices as integrated circuits and present approaches such as hybrid inductive-capacitive converter topologies which can enable further integration at the cost of increased complexity. The associated tradeoffs will be discussed.

#### Bio

Giovanni Frattini received his MS degree in electronic engineering from U. of Pavia in 1997. The same year he joined STMicroelectronics in Milan, Italy, as an Analog Designer in the BCD technology R&D, where he worked on designing signal analog circuitry for smart power chips, data converters, HV linear and DC/DC power converters. Joined National Semiconductor (now Texas Instruments) in 2008 to start and lead the R&D team in the Design Center located in Milan, Italy, currently responsible for the R&D teams in Italy and Germany for power management applications.

His current research interests include fully integrated power converters, high voltage applications, high frequency switching power conversion, isolated power converters.

CIAN O'MATHUNA

11.30 - 12.30

## Making Magnetics Disappear Integrated Magnetics for Power Management

### Abstract

The work-horse of power management, the dc-dc switched-mode converter, can deliver high-efficiency power to multi-voltage rails in electronic loads such as microprocessors and to multiple peripherals in portable electronics such as screens, cameras and audio units. One of the major drawbacks of existing dc-dc converter technology is the need for off-chip capacitors and bulky inductors for energy storage and filtering. These passive components take up significant space, and profile, on the electronics motherboard, add to the cost of the bill of materials and can impact on the overall system performance.

Moving to very high frequency (in the 20 to 200MHz range) magnetic inductors and transformers for dc-dc converters allows the inductance values to be reduced enabling dramatic miniaturisation of the magnetics and the overall converter footprint and profile. This miniaturisation can be enabled by thin film 'magnetics-on-silicon' technology.

This tutorial will discuss the trends in moving to miniaturised power converter platforms. The tutorial will introduce 'magnetics on silicon' and will cover design, thin-film magnetic materials and MEMS fabrication of micro-inductor and micro-transformer components. Fabricated devices will be presented along with the performance of the components in real converters. Finally, a perspective on the future opportunities and challenges will be discussed.

### Bio

Prof. Ó Mathúna is Head of Strategic Programmes at Tyndall National Institute, University College Cork, Ireland. His research is focused on making and powering the smart things for the Internet of Everything. He is co-author of more than 200 publications and has 30+ years in research/technology transfer to global electronics companies. In 2005, he was co-founder of the industry/academic group, PEIG (Power Electronics Ireland Group). He has been a Director of the PSMA (US-based Power Sources Manufacturers Association) and co-chair of its Packaging Committee. In 2008, he founded the International Workshop on Power Supply-on-Chip (PwrSoC), the global flagship for PSMA and the IEEE Power Electronics Society. In 2013, he was named IEEE Fellow in the field of power electronics "for leadership in the development of power supply using micromagnetics on silicon".

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**LUNCH**  
12.30 - 14.00

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**STEFANO STANZIONE**  
14.00 - 15.00

## **Vibrational harvesters for wireless sensing applications**

### **Abstract**

Wireless sensing is a promising technique for sensing the state of moving parts in industrial and automotive applications, allowing improvements of safety and reliability. Unfortunately, the best place for sensing is often not the best for wiring power cables. Batteries can solve the energy problem, but their periodic recharge or replacement is expensive. This makes energy harvesting from mechanical vibrations a very promising solution. However, multiple challenges will need to be solved to make these solutions practical. A successful product should combine low-power sensor and power management designs and efficient harvester interface. Additionally, the system will need to be effective despite the variations in time of available power.

### **Bio**

Stefano Stanzione received the M.S. degree in electrical engineering and the Ph.D. degree from the University of Pisa, Pisa, Italy, in 2006 and 2010, respectively. His Ph.D. work focused on the analog building blocks of autonomous UHF RFID tags. He joined the Holst Centre/imec, Eindhoven, The Netherlands, in 2010, where he is currently an Analog Design Engineer. His current research interests include ultralow-power circuits for energy harvesting and battery management. Dr. Stanzione has been a member of the Analog Technical Program Sub-Committee of ISSCC since 2014.

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**COFFEE BREAK**  
15.00 - 15.30

## BERNHARD WICHT

15.30 - 16.30

**Power Management Design  
for Highly Integrated Automotive ICs****Abstract**

With the adoption of more electronics, vehicles become safer, cleaner, more comfortable, and more affordable and will soon support autonomous driving. Overall system size and cost require highly integrated power management solutions. With the introduction of the 48V board net in addition to the conventional 12V battery, there is an increasing need for point-of-load converters that can handle high input voltages. The high-voltage electrical drive train (400V) demands for galvanic isolated and highly integrated gate drivers for signal and power transfer. This talk gives a general introduction into circuit and system design for high-Vin DCDC converters and gate drivers for automotive applications. A particular focus will be on concepts and trends towards higher integration. This includes fast switching, which scales down the size of passive components. Moreover, digital control loops eliminate external passive components and provide flexibility as well as performance advantages over conventional analog control. The concept of high-voltage charge and energy storing enables area-efficient gate driver designs with a minimum of external components.

**Bio**

Bernhard Wicht received the Dipl.-Ing. degree in electrical engineering from University of Technology Dresden, Germany, in 1996 and the Ph.D. degree from University of Technology Munich, Germany, in 2002. Between 2003 and 2010, he was with the Mixed-Signal Automotive business unit of Texas Instruments in Freising, Germany, responsible for the design of automotive ICs for power management, motor control and transceivers. Between 2010 and March 2017, he was a full professor for integrated circuit design and a member of the Robert Bosch Center for Power Electronics at Reutlingen University, Germany. In April 2017, he became the head of the Mixed-Signal IC Design group at Leibniz University Hannover, Germany. His research interest includes power management and gate driver IC design.

## 1 kV on-chip, hard to resist?

### Abstract

This tutorial focuses on the design issues of ultra high voltage (up to 1000 V), high-power integrated circuit design. The speaker will discuss the complete design flow of a high voltage design case. In the first part, some technological aspects are discussed, such as parasitic coupling, shielding, oxide trenches, etc. Afterwards, several circuit solutions to cope with high-voltage transients are presented and discussed into detail. Special attention will go to simulation issues in high-voltage design. The next step in the design process is layout; as can be expected, several specific DRC rules need to be taken into account to obtain a working design, without the risk of early breakdown. DRC tools are a great help to obtain a working layout, however, they are only as smart as the person who implemented or uses them. Finally, also issues as packaging, heat dissipation and testing will be discussed. It is clear that special packaging techniques are required to handle these high voltages and high power dissipation, not to mention the increased risk for the test engineer.

### Bio

Valentijn De Smedt (S'08) was born in Lubbeek, Belgium, in 1984. He received the M.Sc. degree in electrical engineering from the Katholieke Universiteit Leuven in 2007. From 2007 to 2014 he was working as a research assistant at the MICAS laboratories of the Katholieke Universiteit Leuven towards a PhD degree on the design of ultra-low-power time-based building blocks for wireless sensor networks, which he received in April 2014. Since 2014 he is employed at MinDCet as a Senior Design Engineer. At MinDCet his focus is on the development of high-voltage ( $> 500\text{V}$ ), high-power ( $> 1\text{kW}$ ) radiation hardened motor drivers and power converters. Since September 2016 he is part-time post-doctoral researcher at the KU Leuven technology campus in Geel.

All tutorials will be held on Monday 11 September.  
08.00 - 09.00 Registrations

**- THE HIDDEN CHALLENGES OF 5G -**  
Tutorial Organizer: Fredrik Tillman, Ericsson Research  
Room **AV 03.12**

**YAO-HONG LIU**  
09.00 - 10.00

## **What is required of 5G to make it attractive for MTC?**

### **Abstract**

In this tutorial, several IoT wireless standards for machine type communication (MTC) will be reviewed. The baseline 5G radio performance that is needed to compete with these IoT standards will be discussed, including an analysis of the battery energy consumption of an MTC device. Finally, the design challenge of the RF transceiver for 5G MTC, such as CMOS PA integration, will be addressed with few subGHz IoT transceivers as case study.

### **Bio**

Yao-Hong Liu (S'04-M'09) received his Ph.D. degree from National Taiwan University, Taiwan, in 2009. He joined Terax Communication, VIA technology, and mobile devices, Taiwan, from 2002 to 2010. Since 2010, he joined imec, the Netherlands. His current research focuses on the ultra-low power and highly digitally-assisted RF transceivers for wireless healthcare and Internet-of-Things (IoT) applications. He currently serves as a technical program committee of the IEEE RFIC symposium.

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**COFFEE BREAK**  
10.00 - 10.30

**Programmable mm-Wave Transmitters:  
Generalized PA Architectures for Frequency  
and Back-off Reconfigurability****Abstract**

The evolution of 5G and future standards are expected to open up several disjointed frequency bands in the mm-Wave frequency range, giving us access to a spectrum with a collective span that is orders of magnitude larger than we had at any point in our history. Future wireless communication architectures need to be designed to allow optimally efficient use of these available spectral resources. Evidently to serve across the disjointed bands spreading across 70-100 GHz in future, deploying large-scale MIMO arrays with dedicated, multiple, narrow-band Tx-Rx architectures becomes inefficient and non-scalable. In this talk, we will present our approaches towards a transmitter and power amplifier architecture that can be reconfigured to operate near optimally over a large chunk of the mm-Wave spectrum. Frequency-reconfigurable integrated mm-Wave transmitters with high power and high back-off efficiency is a hard problem. In this talk, we will present a systematic methodology that allows impedances to be synthesized dynamically for both frequency and back-off reconfigurability by exploiting interactions of multiple digital PA cells in a general multi-port network. With the ultimate aim of an universal front-end, we present a systematic methodology for synthesis of this reconfigurable architecture that loosens the classical trade-offs between output power, efficiency, spectral efficiency (linearity) and spectral reconfigurability.

**Bio**

Dr. Kaushik Sengupta received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from the Indian Institute of Technology (IIT), Kharagpur, India, both in 2007, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2008 and 2012, respectively. In 2013, he joined the faculty of the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA.

He received the Young Investigator Program Award from Office of Naval Research in 2017 and two time inductee into 'Princeton Engineering Commendation List for Outstanding Teaching'. He was the recipient of the Charles Wilts Prize in 2013 from Caltech for the best Ph.D. thesis in Electrical Engineering in 2012, the Caltech Institute Fellowship and the Prime Minister Gold Medal Award of IIT (2007). He serves on the Technical Program Committee of IEEE Custom Integrated Circuits conference and European Solid-state Circuits Conference. He was the recipient of the IBM Ph.D. fellowship (2011), the IEEE Solid-State Circuits Society Pre-doctoral Achievement Award (2012), the IEEE Microwave Theory and Techniques Graduate Fellowship (2012), and the Analog Devices Outstanding Student Designer Award (2011). He was the co-recipient of the IEEE RFIC Symposium Best Student Paper Award in 2012 and 2015 Microwave Prize from IEEE Microwave Theory and Techniques Society for the most influential paper in the field of interest to IEEE MTT-S society in 2013.

## LIESBET VAN DER PERRE

11.30 - 12.30

## Implementing Massive MIMO systems: coarse processing gives fine performance

### Abstract

Massive MIMO opens up a new dimension of wireless communications by using an excess of base-station antennas, relative to the number of active terminals. The technique has been demonstrated to achieve a record spectral efficiency through very efficient spatial multiplexing, attainable using linear processing in a time-division duplex mode. The concept through the excess of antennas can also realize radical improvements in energy efficiency, making it a key candidate technology for 5G wireless systems.

Essential to achieve the gains in practise, is the ability to realize the many antenna paths at low complexity. In this lecture we will zoom in on the implementation of Massive MIMO systems, and demonstrate that coarse processing can give fine performance. Specific aspects that will be handled include:

- Introduction to the Massive MIMO concepts.
- Power consumption and complexity breakdown of Massive MIMO systems.
- Exploiting system concepts for low complexity processing.
- Analog processing requirements: relaxing PA and convertor designs and power consumption.
- Efficient DSP for many antenna paths: Algorithm-architecture-circuit co-design.
- A perspective on lean terminals.

An overall status of Massive MIMO technology will be provided. The main challenges to be resolved in order to pave the way for actual deployment will be highlighted.

### Bio

Liesbet Van der Perre received the M.Sc. and PhD degree in Electrical Engineering from the KU Leuven, Belgium, in 1992 and 1997 respectively. She was appointed honorary doctor at Lund University, Sweden, in 2015. She joined imec's wireless group in 1997 and took up responsibilities as senior researcher, system architect, project leader and program director, until 2015. She was appointed Professor at the Electrical Engineering Department of KU Leuven in 2016. Liesbet is a (co-)author of over 300 scientific publications. She is the scientific leader for the FP7-MAMMOET project. Prof. Van der Perre is member of the Board of Directors of Zenitel and guest Professor at the University of Lund.

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**LUNCH**  
12.30 - 14.00

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**BRAM NAUTA**  
14.00 - 15.00

**Integrated wide-band baseband filters  
and narrow-band RF filters for 5G**

**Abstract**

Future 5G communications will operate at mm wave RF frequencies where wide band channels are available. This implies that the “baseband” filters for channel selection and anti-aliasing will have bandwidths in the order of a GHz. Given the fact that the building blocks of those filters need to be a factor 100 faster, this places serious design challenges on these circuits.

Also on the RF receiver side, there is a desire to have narrow band selectivity in order to remain interferer robust. Recently, N-path filters and mixer-first receivers have demonstrated that frequency translated filtering can combine a high linearity with low noise and frequency tuneability over a wide range of RF frequencies.

This tutorial will cover the basics of analog filters: synthesis, fundamental trade-offs in power dissipation, SNR, Q, and operating frequency. Also for frequency translated narrow band RF filters the basics and fundamentals are explained. The tutorial will be illustrated with several implementation examples.

**Bio**

Bram Nauta received the M.Sc. and Ph.D. degrees from the University of Twente, Enschede, The Netherlands in 1987 and 1991 respectively. After that he joined Philips Research laboratories in Eindhoven the Netherlands. In 1998, he returned to the University of Twente, where he is currently a distinguished professor, heading the IC Design group and chair of the EE department. He served as the Editor-in-Chief (2007-2010) of the IEEE Journal of Solid-State Circuits (JSSC), and was the 2013 program chair of the International Solid State Circuits Conference (ISSCC). He is IEEE fellow and currently the president elect of the IEEE Solid-State Circuits Society.

**COFFEE BREAK**

15.00 - 15.30

**CHRISTIAN FAGER**

15.30 - 16.30

**Challenges in 5G transmitter design****Abstract**

This talk will give an overview to some of the new challenges that will drive the development of transmitters in 5G systems and beyond. Massive multi-antenna transmitter architectures and millimeter wave frequencies will be key technology ingredients to facilitate the dramatic improvements in capacity, energy efficiency and reliability needed.

As we will discuss in this talk, this paradigm shift will force us to revisit the fundamental linearity and efficiency tradeoffs that typically dictate the design of transmitters in general and power amplifiers in particular. Focusing on millimeter wave silicon CMOS and BiCMOS transmitter circuit realizations, promising power amplifier circuit and transmitter architectures will therefore be reviewed in the context of 5G requirements.

Further challenges arise when these transmitter circuits are implemented as part of a low-cost highly integrated multi-antenna package. We will present a new system simulation framework that enables an accurate prediction of the joint nonlinear effects of circuit-, antenna-, and thermal design. Different phased array and massive MIMO transmitter examples will illustrate typical applications and the importance of co-design in highly integrated 5G transmitters.

**Bio**

Prof. Christian Fager received his M.Sc. and Ph.D. degrees from Chalmers University of Technology, Sweden, in 1998 and 2003, respectively. Since 2015 he is a Professor at the Microwave Electronics Laboratory at the same university. Dr. Fager has authored and co-authored more than 100 papers in international journals and conferences. His research focuses on design, characterization and modelling of energy efficient and linear transmitter circuits for future wireless communication and sensor systems. Dr. Fager is currently an Associate Editor of IEEE Microwave Magazine.

## Opto implementation challenges for 5G networks

### Abstract

Silicon Photonics is recognized to be the technology best suitable to develop high scale integration optical system on chip.

The exploitation of the same highly developed CMOS manufacturing infrastructure and material used for electronic integrated circuits should ensures low cost and mass-manufacturability. The energy-efficient physical mechanisms used to process high capacity optical data flows, the small dimensions of the photonic circuits made possible by the high refractive index contrast of silicon photonics and the tight integration of photonic with the control electronic, allowed by the use of the same production technologies, should ensure low power consumption.

The characteristics of this technology, the strengths and weakness are discussed. The status of development for both commercial devices and experimental prototypes are reported. The challenges to be overcome in the near future, for the exploitation of the full potential of this technology and for extending the range of application of photonics, are also discussed.

The recent advancements achieved in the realization of high scale photonic integrated circuits could drive the introduction of optical switching and networking in new application areas where these functions could be advantageously exploited but this is prevented by the cost and footprint of conventional optical technologies based on discrete components. New optical system for radio access and data centers applications will be presented and discussed together with the enabling silicon photonics integrated devices. Finally, future perspectives and research directions are given.

### Bio

Francesco Testa is a Principal Researcher at Ericsson Research in Pisa, Italy, focusing on photonics integrated technologies and their system applications. He started working in 1985 at Alcatel FACE Research Center in Rome, investigating coherent optical networks and related technologies. He joined Ericsson in 1991 to work on the first demonstrations of WDM optical transport systems, and later in optical networks architectures and technologies research, followed by several years spent on design of HW circuits and systems for SDH, ATM, LMDS, GSM, DECT and Narrowband Access. Francesco received his degree in Electronic Engineering, summa cum laude, from the University of Rome.

All workshops will be held on Monday 11 September.

## CONNECT

Room **AV 04.17**

### Abstract

The workshop will provide technical information about emerging interconnect technologies, with the focus on Carbon Nanotubes (CNT). A broad overview of all the major aspects of CNT interconnects will be offered, ranging from the innovative growth/deposition techniques of local and global lines to the novel measurement and simulation methodologies developed to characterize CNT performances. The core of the workshop will be based on the latest results arising from the research within the H2020 EU-funded project CONNECT. Invited talks from academia, research centers and industry will enrich the global perspective of the workshop.

### Target Audience

The target audience is students, researchers, engineers and entrepreneurs who have an interest or work in the areas related to advanced and future interconnects for integrated circuits. Since interconnects delay is a major limitation to circuits performance, anyone interested in advanced CMOS technologies will benefit from the topics addressed by the workshops' talks. Researchers working in the field of Carbon Nanotubes, even if not for with direct application in interconnects technology, will also find cross-disciplinary interest in this workshop. Finally, CMOS circuit designers will be able to gather useful information on modeling, design and optimization opportunities offered by Carbon Nanotubes based technologies.

### Background on CONNECT Project

#### CarbON Nanotube composite Interconnects

As the chip size goes down, interconnects become major bottlenecks irrespective of the application domain due to electromigration issues and an ever-increasing power consumption. The CONNECT project investigates ultra-fine CNT lines and metal- CNT composite material for addressing the issues of current state-of-the-art copper interconnects. Novel CNT interconnect architectures for the exploration of circuit- and architecture-level performance and energy efficiency will be developed. CMOS compatibility as well as challenges of transferring new processes into industrial mass production will be addressed. The members of the CONNECT consortium from Germany, Switzerland, Great Britain and France are embedded along the electronics value chain from fundamental research to end-users and bring together some of the most renowned research groups in that field in Europe. With significantly improved

electrical resistivity, ampacity, thermal and electromigration properties of CNT interconnects compared to state-of-the-art approaches for conventional copper interconnects, an increased power and scaling density of CMOS or CMOS extension will be available and applicable to alternative computing schemes such as neuromorphic computing. The technologies developed in this project are key for both performance and manufacturability of scaled microelectronics to manifest miniaturized microelectronic products with enhanced functionality at ever decreasing cost. The procurement of CONNECT will foster the recovery of market shares of the European electronic sector and prepare the industry for future developments of the electronic landscape. You can find more information about CONNECT project at the website [www.connect-h2020.eu](http://www.connect-h2020.eu).

## Program

8.00	<b>Arrival &amp; Registration</b>
8.30	<b>Welcome and CONNECT Open Day Introduction</b> Prof. Aida Todri-Sanial, Dr. Salvatore M. Amoroso (Organizers)
8.45	<b>Overview of the EC H2020 CONNECT project</b> Dr. Benjamin Uhlig (Fraunhofer-Dresden)
9.00	<b>Highly Energy-Efficient Digital NanoSystems: New Logic, Memory, Interconnects, &amp; 3D integration</b> Dr. Gage Krieger Hills (Stanford University)
9.35	<b>Direct, dry deposition of high quality SWNT thin films</b> Prof. Esko Kauppinen (Aalto University)
10.10	<b>Coffee Break</b>
10.40	<b>Doped CNTs for advanced local interconnects</b> Dr. Jean Dijon (CEA-Grenoble)
11.15	<b>CNT-metal-composites for global interconnects</b> Dr. Benjamin Uhlig (Fraunhofer-Dresden)
11.50	<b>Vertical Multi-walled CNT interconnects evaluation at full wafer level</b> Dr. Marleen van der Veen (imec)
12.30	<b>Lunch Break</b>
14.00	<b>Heterogeneous integration of low-dimensional nanomaterials</b> Dr. Shu-Jen Han (IBM TJ Watson)
14.35	<b>Manufacturability of CNT interconnects</b> Dr. Bingan Chen (AIXTRON-UK)
15.10	<b>Coffee Break</b>
15.40	<b>Thermal and Electrical Characterization of CNTs interconnects</b> Dr. Bernd Gotsmann (IBM-Zurich)
16.15	<b>Hierarchical multi-physics simulation of CNT interconnects</b> Prof. Aida Todri-Sanial (CNRS-Montpellier)
16.50	<b>Wrap Up &amp; Closure</b>

All workshops will be held on Monday 11 September.

**MOS-AK**  
**Modeling of Systems and Parameter**  
**Extraction Working Group**  
Room **AV 91.12**

The MOS-AK is a HiTech forum to discuss the frontiers of electron device modeling with emphasis on simulation-aware models. The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

**[WWW.MOS-AK.ORG/LEUVEN\\_2017](http://WWW.MOS-AK.ORG/LEUVEN_2017)**

**Extended MOS-AK Committee**

International MOS-AK Board of R&D Advisers

- Larry Nagel, Omega Enterprises Consulting (US)
- Andrei Vladimirescu, UCB (US); ISEP (FR)

**MOS-AK Workshop Program Coordination**

- Jean-Michel Sallese, EPFL (CH)
- Daniel Tomaszewski, ITE (PL)
- Wlodek Grabinski, MOS-AK (EU)

**MOS-AK Technical Committee**

- [www.mos-ak.org/committee.html](http://www.mos-ak.org/committee.html)

## Program

- 8.00 **Arrival & Registration**
- 8.30 **MORNING SESSIONS**
- **ASCENT: Access to Leading European Nanoelectronics Technology**  
Jim Greer, Tyndall (IRL)
  - **Junctionless Nanowire Transistors Performance: Static and Dynamic Modeling**  
Marcelo Pavanello, FEI (BR)
- 10.00 **Coffee Break**
- 10.30 **MORNING SESSIONS (continued)**
- **Modeling and Analysis of Full-Chip Parasitic Substrate Currents**  
Wim Schoenmaker, Magwel (B)
  - **Small- and large-signal RF modeling of silicon-based substrates**  
Jean-Pierre Raskin, UCL (B)
  - **Spice modeling of beyond CMOS**  
Chika Tanaka, Toshiba (J)
- 12.30 **Lunch**
- 14.00 **AFTERNOON SESSIONS**
- **ASCENT Open Access to 14nm PDKs**  
Nicolas Cordero, Tyndall (IRL)
  - **Modelling of Surface Traps Effect on Semiconductor Nanowires**  
Ashkhen Yesayan, IRPhE (AM)
- 15.00 **Coffee Break**
- 15.30 **AFTERNOON SESSIONS (continued)**
- **Measurement and modelling of specific behaviors in 28nm FD SOI UTBB MOSFETs of importance for analog / RF amplifiers**  
Denis Flandre, UCL (B)
  - **IEEE EDS Compact Model Standardization**  
Benjamin Iniguez URV (SP)
  - **3D electromagnetic simulation and QUCS modeling of split ring resonators**  
Saravana Maruthamuthu, QUCS (D)
- 17.00 **Closure**

All workshops will be held on Monday 11 September.

**SEMICONDUCTOR MEMORIES:**  
**the follow-up of a successful story**

Room **AP 01.30**  
(Auditorium Jean Monnet)

**Organizer**

Prof. Francisco Gamiz

Universidad de Granada & REMINDER Project

**Abstract**

In 1968, Dr. Robert Dennard from IBM introduced the concept of Dynamic Random Access Memory (DRAM) cell, which consists in a transistor (1T) and a capacitor (1C) where the information is stored. Since its introduction almost 50 years ago, this memory cell has been present in all electronic devices up to now. However, the arrival of the Internet of Things (IoT) and the requirement of ultra-low power consumption and extremely cheap devices are making developers to reconsider their design goals, by using memory in new and innovative ways. In many cases, this involves using new, or less familiar, memory technologies and examining memory much earlier in their design cycles. The vast majority of embedded memories are currently charged based (DRAM, FLASH) or flip-flop based (SRAM), the last one penalized by its huge area consumption. The other alternative storage options (which are not yet mature from a commercial perspective) can be grouped into three categories, ReRAM (resistive) or MRAM (magnetic), and body-charged memories (so called floating-body DRAMs, FB-DRAM). All these memory approaches will be analyzed by well-known experts in the field both from Industry and Academia.

## Program

8.30	<b>Welcome Introduction</b> Prof. Francisco Gamiz (Unversidad de Granada, REMINDER project)
9.00	<b>MRAM solutions</b> Dr. Kilho Lee (MRAM Team, Samsung Electronics, Korea)
9.45	<b>FDX12 technology and embedded NVM solutions for IoT</b> Dr. Manfred Horstman (Global Foundries, Dresden, Germany)
10.30	<b>Resistive memories for spike-based neuromorphic circuits</b> Dr. Elisa Vianello (CEA, France)
11.15	Coffee Break
11.45	<b>Stand-alone DRAM memory status and challenges</b> Dr. Pierre Fazan (Micron Europe, Leuven, Belgium)
12.30	<b>MRAM developments at IBM</b> Dr. Guohan Hu (IBM Yorktown Heights, New York, USA)
13.15	Lunch
14.30	<b>FDSOI technology for IoT applications</b> Dr. Philippe Galy (STMicroelectronics)
15.00	<b>Z2FET memory for low-power applications</b> Prof. Sorin Cristoloveanu (IMEP-MINATEC, Grenoble France)
15.30	<b>Modelling of Z2FET memory cell</b> Dr. Joris Lacord (CEA-LETI, Grenoble)
16.00	Coffee Break
16.30	<b>Variability of Z2FET memory cells and matrix</b> Prof. Asen Asenov (Glasgow and Synopsys U.K.)
17.00	<b>Circuit \design with Z2FET memory cell for low-power applications</b> Dr. Andy Pickering (Surecore U.K.)
17.30	Conclusions

All workshops will be held on Monday 11 September.

**SINANO-NEREID**  
**Towards a new NanoElectronics**  
**Roadmap for Europe**  
Room **AP 00.15**  
(Auditorium Max Weber)

**Organizers**

Francis Balestra, Grenoble INP-CNRS (NEREID Coordinator),  
Enrico Sangiorgi, SiNANO Institute/IUNET (SiNANO Institute  
Director), Ralf Popp, Edacentrum (NEREID Dissemination  
Manager)

**Abstract**

Within this Workshop the H2020 Coordination and Support Action NEREID entitled “NanoElectronics Roadmap for Europe: Identification and Dissemination” (<https://www.nereid-h2020.eu/>, n° 685559) will report on its recent findings on the way to map the future of European Nanoelectronics. The objective of this 3 year project NEREID is to elaborate a new NanoElectronics Roadmap for Europe using a pretty new method: starting from the needs of applications and leveraging the strengths of the European eco-system the advanced design and technology concepts are examined with respect to their potential to serve future application needs and/or to lead to possible disruptive applications. Focusing on a longer term time horizon, NEREID will lead to an application oriented early benchmark/identification of promising novel nanoelectronic technologies, and an identification of bottlenecks all along the innovation (value) chain.

In this workshop, which is supported by the European Institute of Nanoelectronics SiNANO ([www.sinano.eu](http://www.sinano.eu)) the NEREID project will report on its recent findings and will bring them into a hopefully vivid feedback situation with the audience, aiming to verify the current results by discussing especially controversial points. Besides applications like automotive, energy, health, IoT and many others, the topics of NEREID and the workshop comprise Beyond CMOS technologies, advanced logic and connectivity, functional diversification, system design and heterogeneous integration as well as equipment and manufacturing science.

## Program

9.00	<b>Welcome</b>	Enrico Sangiorgi (SINANO Institute)
9.05	<b>"Presentation of the NEREID Project"</b>	Francis Balestra (Grenoble INP/CNRS)
9.25	<b>"European Status, Vision and Perspectives in Nanoelectronics"</b>	Francisco Ibanez (European Commission)
10.00	<b>"Emerging technologies for Beyond CMOS"</b>	Jouni Ahopelto (VTT)
	<b>"Alternative Computing Paradigms"</b>	Clivia Sotomayor Torres (ICN2)
10.45	<b>Coffee Break</b>	
11.00	<b>"Advanced logic: Nanoscale FET"</b>	Anda Mocuta (imec)
	<b>"RF and mmW Design/Connectivity"</b>	Yann Deval (IMS Bordeaux)
11.45	<b>Functional Diversification:</b>	
	<b>"Smart Sensors"</b>	Montserrat Fernandez-Bolanos (EPFL)
	<b>"Smart Energy Devices"</b>	Steve Stoffels (imec)
	<b>"Energy for Autonomous Systems"</b>	Stéphane Monfray (ST Microelectronics)
12.45	<b>Lunch</b>	
14.00	<b>"System Design"</b>	Danilo Demarchi (Politecnico Di Torino) Holger Schmidt (Infineon)
	<b>"Heterogenous Integration"</b>	Georgios Fagas (Tyndall)
14.45	<b>"Equipment and Manufacturing Science"</b>	Thanasis Dimoulas (NCSRDI)
15.30	<b>Conclusions</b>	Enrico Sangiorgi (SINANO Institute)

## Tuesday, September 12

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## Tuesday, September 12

### Joint Plenary 1: Françoise Chombar, Melexis - Engineering a Safe, Clean & Comfortable Future

Session Code: A1L-A  
Location: Vesalius  
Time: 09:00 - 09:40  
Chair(s): Georges Gielen; *KU Leuven*

**09:00 Engineering a Safe, Clean & Comfortable Future**  
Françoise Chombar  
*Melexis, Belgium*

### Joint Plenary 2: Peter Real, Analog Devices - Navigating without a Moore's Law Compass

Session Code: A2L-A  
Location: Vesalius  
Time: 09:40 - 10:20  
Chair(s): Georges Gielen; *KU Leuven*

**09:40 Navigating Without a Moore's Law Compass**  
Peter Real  
*Analog Devices Inc, Ireland*

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## Tuesday, September 12

### References

Session Code: A3L-B  
Location: AP00.15  
Time: 11:00 - 12:20  
Chair(s): Peter Mole; *Intersil*  
Marco Berkhout; *NXP*

- 11:00 A Frequency-Locked Loop Based on an Oxide Electrothermal Filter in Standard CMOS**  
Lorenzo Pedalà, çağrı Gürleyük, Sining Pan, Fabio Sebastiano, Kofi Makinwa  
*Delft University of Technology, Netherlands*
- 11:20 A Compact Programmable Differential Voltage Reference with Unbuffered 4 mA Output Current Capability and  $\pm 0.4\%$  Untrimmed Spread**  
Simone Del Cesta<sup>3</sup>, Andrea Ria<sup>2</sup>, Roberto Simmarano<sup>2</sup>, Massimo Piotto<sup>1</sup>, Paolo Bruschi<sup>3</sup>  
<sup>1</sup>IEIT-CNR - Pisa, Italy; <sup>2</sup>Sensichips srl, Italy; <sup>3</sup>University of Pisa, Italy
- 11:40 A 420 fW Self-Regulated 3T Voltage Reference Generator Achieving 0.47%/V Line Regulation from 0.4-to-1.2 V**  
Hui Wang, Patrick Mercier  
*University of California, San Diego, United States*
- 12:00 A 1.02nW PMOS-Only, Trim-Free Current Reference with 282ppm/°C from -40°C to 120°C and 1.6% Within-Wafer Inaccuracy**  
Qing Dong, Inhee Lee, Kaiyuan Yang, David Blaauw, Dennis Sylvester  
*University of Michigan, Ann Arbor, United States*

## Tuesday, September 12

### RF Receivers and Detectors

Session Code: A3L-C  
 Location: AV91.12  
 Time: 11:00 - 12:20  
 Chair(s): Marc Tiebout; *Infineon*  
 Andrea Neviani; *Università degli studi di Padova*

- 11:00 A Noise-Efficient, In-Pixel Readout for FET-Based THz Detectors with Direct Incremental A/D Conversion**  
 Moustafa Khatib, Matteo Perenzoni, David Stoppa  
*Fondazione Bruno Kessler, Italy*
- 11:20 A 0.7-2 GHz Auxiliary Receiver with Enhanced Compression for SAW-Less FDD**  
 Daniele Montanari<sup>2</sup>, Danilo Manstretta<sup>2</sup>, Rinaldo Castello<sup>2</sup>, Gerardo Castellano<sup>1</sup>  
<sup>1</sup>*University of Napoli Federico II, Italy*; <sup>2</sup>*University of Pavia, Italy*
- 11:40 A HBT-Based 300MHz-12 GHz Blocker-Tolerant Mixer-First Receiver**  
 Robin Ying<sup>1</sup>, Matthew Morton<sup>2</sup>, Alyosha Molnar<sup>1</sup>  
<sup>1</sup>*Cornell University, United States*; <sup>2</sup>*Raytheon, United States*
- 12:00 A 400 MHz 4.5 nW -63.8 dBm Sensitivity Wake-Up Receiver Employing an Active Pseudo-Balun Envelope Detector**  
 Po-Han Peter Wang, Haowei Jiang, Li Gao, Pinar Sen, Young-Han Kim, Gabriel Rebeiz, Patrick Mercier, Drew Hall  
*University of California, San Diego, United States*

## Tuesday, September 12

### Digital Accelerators

Session Code: A3L-D

Location: AV01.12

Time: 11:00 - 12:20

Chair(s): Andreas Burg; École polytechnique fédérale de Lausanne  
Tobias Noll; *Rheinisch-Westfälische Technische Hochschule Aachen*

**11:00 A 3-GHz Reconfigurable 2/3-Level 96/48-Channel Cross-Correlator for Synthetic Aperture Radiometry**

Erik Ryman<sup>1</sup>, Anders Emrich<sup>2</sup>, Lars Svensson<sup>1</sup>, Per Larsson-Edefors<sup>1</sup>

<sup>1</sup>*Chalmers University of Technology, Sweden*; <sup>2</sup>*Omnisys Instruments AB, Sweden*

**11:20 Accuracy/Energy-Flexible Stochastic Configurable 2D Gabor Filter with Instant-on Capability**

Naoya Onizawa<sup>2</sup>, Kazumichi Matsumiya<sup>2</sup>, Warren Gross<sup>1</sup>, Takahiro Hanyu<sup>2</sup>

<sup>1</sup>*McGill University, Canada*; <sup>2</sup>*Tohoku University, Japan*

**11:40 A 0.17-mm<sup>2</sup> 3.19-nJ/Transform 256-Point Fast Fourier Transform Core Based on Spatiotemporally Fine-Grained Active Leakage Suppression**

Joao Pedro Cerqueira, Mingoo Seok

*Columbia University, United States*

**12:00 Improved Power Side Channel Attack Resistance of a 128-Bit AES Engine with Random Fast Voltage Dithering**

Arvind Singh<sup>1</sup>, Monodeep Kar<sup>1</sup>, Sanu Mathew<sup>2</sup>, Anand Rajan<sup>2</sup>, Vivek De<sup>2</sup>, Saibal Mukhopadhyay<sup>1</sup>

<sup>1</sup>*Georgia Tech, United States*; <sup>2</sup>*Intel Corporation, United States*

## Tuesday, September 12

### Optical Sensors

Session Code: A3L-E

Location: AV03.12

Time: 11:00 - 12:20

Chair(s): Robert Henderson; *University of Edinburgh*  
Matteo Perenzoni; *Fondazione Bruno Kessler*

**11:00 A <25 uW CMOS Monolithic Photoplethysmographic Sensor with Distributed 1b Delta-Sigma Light-to-Digital Convertor**

Hyung-Gi Kim, Dong-Woo Jee  
*Ajou University, Korea*

**11:20 An 80 X 25 Pixel CMOS Single-Photon Range Image Sensor with a Flexible on-Chip Time Gating Topology for Solid State 3D Scanning**

Henna Ruokamo, Lauri Hallman, Harri Rapakko, Juha Kostamovaara  
*University of Oulu, Finland*

**11:40 Pixel Array with 5x5 Spatial Highpass Filter for a Retinal Implant**

Henning Schütz, Stefan Gambach, Hans Kaim, Albrecht Rothermel  
*University of Ulm, Germany*

**12:00 A Sun Sensor Implemented with an Asynchronous Luminance Vision Sensor**

Juan Antonio Leñero-Bardallo<sup>1</sup>, Lukasz Farian<sup>2</sup>, José María Guerrero-Rodríguez<sup>1</sup>, Ricardo Carmona-Galán<sup>3</sup>, ángel Rodríguez-Vázquez<sup>3</sup>

<sup>1</sup>*University of Cádiz, Spain*; <sup>2</sup>*University of Oslo, Norway*;

<sup>3</sup>*University of Seville, Spain*

## Tuesday, September 12

### Amplifiers and Comparators

Session Code: A4L-B  
Location: AP00.15  
Time: 14:00 - 15:20  
Chair(s): Pieter Harpe; *TU Eindhoven*  
Kimmo Koli; *Ericsson*

- 14:00 A 30fJ/Comparison Dynamic Bias Comparator**  
Harijot Singh Bindra, Chris E. Lokin, Anne-Johan Annema, Bram Nauta  
*University of Twente, Netherlands*
- 14:20 A 1.6 $\mu$ W Tunable Organic Transimpedance Amplifier for Photodetector Applications Based on Gain-Boosted Common-Gate Input Stage and Voltage-Controlled Resistor with  $\pm 0.5\%$  Nonlinearity**  
Samar Elsaegh<sup>2</sup>, Hagen Klauk<sup>1</sup>, Ute Zschieschang<sup>1</sup>, Hans Zappe<sup>2</sup>, Yiannos Manoli<sup>2</sup>  
<sup>1</sup>*Max Planck Institute for Solid State, Germany*; <sup>2</sup>*University of Freiburg - IMTEK, Germany*
- 14:40 A Transimpedance Amplifier Using a Widely Tunable PVT-Independent Pseudo-Resistor for High-Performance Current Sensing Applications**  
Denis Djekic<sup>4</sup>, Georg Fantner<sup>1</sup>, Jan Behrends<sup>2</sup>, Klaus Lips<sup>3</sup>, Maurits Ortmanns<sup>4</sup>, Jens Anders<sup>4</sup>  
<sup>1</sup>*EPFL Lausanne, Switzerland*; <sup>2</sup>*Free University of Berlin, Germany*; <sup>3</sup>*Helmholtz-Zentrum Berlin for Materials and Energy, Germany*; <sup>4</sup>*University of Ulm, Germany*
- 15:00 Push-Pull Amplifier with Constant Transconductance for a Current Sense Application**  
Emiliano Alejandro Puia, Adriano Sambucco  
*Infineon Technologies Austria AG, Austria*

## Tuesday, September 12

### Oscillators

Session Code: A4L-C

Location: AV91.12

Time: 14:00 - 15:20

Chair(s): Jaehyouk Choi; *UNIST*  
Kenichi Okada; *Tokyo Institute of Technology*

- 14:00 A 30-GHz Class-F23 Oscillator in 28nm CMOS Using Harmonic Extraction and Achieving 120 kHz 1/F<sup>3</sup> Corner**  
Yizhe Hu, Teerachot Siriburanon, Robert Bogdan Staszewski  
*University College Dublin, Ireland*
- 14:20 A 21GHz 20.5%-Tuning Range Colpitts VCO with -119 dBc/Hz Phase Noise at 1MHz Offset**  
Fabio Boscolo<sup>2</sup>, Fabio Padovan<sup>1</sup>, Fabio Quadrelli<sup>2</sup>, Marc Tiebout<sup>1</sup>, Andrea Neviani<sup>2</sup>, Andrea Bevilacqua<sup>2</sup>  
<sup>1</sup>*Infineon Technologies Austria AG, Austria*; <sup>2</sup>*University of Padova, Italy*
- 14:40 A 1-MHz On-Chip Relaxation Oscillator with Comparator Delay Cancellation**  
Josip Mikulic<sup>1</sup>, Gregor Schatzberger<sup>1</sup>, Adrijan Baric<sup>2</sup>  
<sup>1</sup>*ams AG, Austria*; <sup>2</sup>*University of Zagreb, Croatia*
- 15:00 A 1.6%/V 124.2 pW 9.3 Hz Relaxation Oscillator Featuring a 49.7 pW Voltage and Current Reference Generator**  
Hui Wang, Patrick Mercier  
*University of California, San Diego, United States*

## Tuesday, September 12

### Wireline and Optical

Session Code: A4L-D

Location: AV01.12

Time: 14:00 - 15:20

Chair(s): Filip Tavernier; *KU Leuven*  
Thomas Toifl; *IBM Zurich Research Laboratory*

**14:00 A 120GHz in-Band Full-Duplex PMF Transceiver with Tunable Electrical-Balance Duplexer in 40nm CMOS**

Niels Van Thienen, Patrick Reynaert  
*KU Leuven ESAT-MICAS, Belgium*

**14:20 A 20Gbps 1.2GHz Full-Duplex Integrated AFE in 28nm CMOS for Copper Access**

Thibaut Gurné<sup>2</sup>, Maarten Strackx<sup>2</sup>, Maarten Tytgat<sup>2</sup>, Jan Cools<sup>1</sup>,  
Patrick Reynaert<sup>1</sup>

<sup>1</sup>*KU Leuven, ESAT-MICAS, Belgium*; <sup>2</sup>*Nokia Bell Labs, United States*; <sup>2</sup>*Nokia Bell Labs, Belgium*

**14:40 Highly Integrated Wavelength-Locked Si Photonic Ring Transmitter Using Direct Monitoring of Drop-Port OMA**

Saurabh Agarwal<sup>3</sup>, Mark Ingels<sup>1</sup>, Marianna Pantouvaki<sup>1</sup>, Michiel Steyaert<sup>2</sup>, Philippe Absil<sup>1</sup>, Joris Vancampenhout<sup>1</sup>

<sup>1</sup>*imec, Belgium*; <sup>2</sup>*KU Leuven, Belgium*; <sup>3</sup>*KU Leuven / imec, Belgium*

**15:00 DDR4 Transmitter with AC-Boost Equalization and Wide-Band Voltage Regulators for Thin-Oxide Protection in 14-nm SOI CMOS Technology**

Marcel Kossel, Christian Menolfi, Pier Andrea Francese, Lukas Kull, Thomas Morf, Thomas Toifl, Matthias Brändli, Alessandro Cevrero, Danny Luu, Ilter Ozkaya, Hazar Yueksel  
*IBM, Switzerland*

## Tuesday, September 12

### ESSCIRC Keynote 1: Yves Baeyens, Nokia Bell Labs: Solving Capacity Bottlenecks in Fixed Access Comms

Session Code: A5L-B  
Location: AP00.15  
Time: 15:50 - 16:30  
Chair(s): Wim Dehaene; *KU Leuven*

**15:50 Solving the Capacity Bottlenecks in Fixed Access Communications**

Yves Baeyens  
*Nokia Bell Labs, United States*

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## Tuesday, September 12

### Energy Harvesting

Session Code: A6L-B

Location: AP00.15

Time: 16:40 - 17:40

Chair(s): Andrei Vladimirescu; *University of California, Berkeley*  
Stefano D'Amico; *Università del Salento*

**16:40 A Piezoelectric Energy Harvester Interface Circuit with Adaptive Conjugate Impedance Matching, Self-Startup and 71% Broader Bandwidth**

Yifeng Cai<sup>2</sup>, Yiannos Manoli<sup>1</sup>

<sup>1</sup>Hahn-Schickard, Germany; <sup>2</sup>IMTEK, University Freiburg, Germany

**17:00 A 2.4μW Input Power Electronic Interface Circuit for Piezoelectric MEMS Harvesters**

Giuseppe Elia Biccario<sup>1</sup>, Massimo De Vittorio<sup>1</sup>, Stefano D'Amico<sup>2</sup>

<sup>1</sup>CBN (Center for Biomolecular Nanotechnologies) - IIT (Istituto Italiano di Tecnologia), Italy; <sup>2</sup>Dipartimento di Ingegneria dell'Innovazione - Università del Salento, Italy

**17:20 A 25 mV-Startup Cold Start System with On-Chip Magnetics for Thermal Energy Harvesting**

Preet Garcha<sup>1</sup>, Dina El-Damak<sup>3</sup>, Nachiket Desai<sup>1</sup>, Jorge Troncoso<sup>1</sup>, Erika Mazotti<sup>2</sup>, Joyce Mullenix<sup>2</sup>, Shaoping Tang<sup>2</sup>, Django Trombley<sup>2</sup>, Dennis Buss<sup>2</sup>, Jeffrey Lang<sup>1</sup>, Anantha Chandrakasan<sup>1</sup>

<sup>1</sup>Massachusetts Institute of Technology, United States; <sup>2</sup>Texas Instruments, United States; <sup>3</sup>University of Southern California, United States

## Tuesday, September 12

### Advanced ADC Techniques

Session Code: A6L-C

Location: AV91.12

Time: 16:40 - 17:40

Chair(s): Klaas Bult; *TU Delft*  
Piero Malcovati; *Università degli Studi di Pavia*

**16:40 A 13mW 64dB SNDR 280MS/s Pipelined ADC Using Linearized Open-Loop Class-AB Amplifiers**

Rohan Sehgal<sup>1</sup>, Frank van der Goes<sup>1</sup>, Klaas Bult<sup>2</sup>  
<sup>1</sup>*Broadcom Ltd, Netherlands*; <sup>2</sup>*Delft University of Technology, Netherlands*

**17:00 A 0.11mm<sup>2</sup> 164dB-FOM 0.18um CMOS Pipelined ADC with Novel Passive Amplification**

Takashi Oshima, Taizo Yamawaki, Koji Maeda  
*Hitachi Ltd., Japan*

**17:20 A CT Delta-Sigma ADC with 9/50MHz BW Achieving 73/71dB DR Designed for Robust Blocker Tolerance in 14nm FinFET**

Francesco Conzatti<sup>1</sup>, Lukas Doerrer<sup>1</sup>, Patrick Torta<sup>1</sup>, Claus Kropf<sup>1</sup>, Dirk Paetzold<sup>1</sup>, Jacinto San Pablo Garcia<sup>2</sup>, Venerando Rallos<sup>2</sup>, Norbert Schembera<sup>2</sup>  
<sup>1</sup>*Intel Austria, Austria*; <sup>2</sup>*Intel Germany, Germany*

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## Tuesday, September 12

### Digital-intensive Frequency Synthesis

Session Code: A6L-D

Location: AV01.12

Time: 16:40 - 17:40

Chair(s): Bogdan Staszewski; *University College Dublin*  
Martin Flatscher; *Infineon Technologies AG*

**16:40 A 14-Bit, 1-ps Resolution, Two-Step Ring and 2D Vernier TDC in 130nm CMOS Technology**

Hechen Wang, Fa Dai

*Auburn University, United States*

**17:00 Quantizer-Less Proportional Path Fractional-N Digital PLL with a Low-Power High-Gain Time Amplifier and Background Multi-Point Spur Calibration**

Minuk Heo<sup>2</sup>, Sunghyun Bae<sup>2</sup>, Jayeol Lee<sup>1</sup>, Cheonsu Kim<sup>1</sup>, Minjae Lee<sup>2</sup>

<sup>1</sup>*Electronics and Telecommunications Research Institute, Korea;*

<sup>2</sup>*Gwangju Institute of Science and Technology, Korea*

**17:20 A 7GS/s Direct Digital Frequency Synthesizer with a Two-Times Interleaved RDAC in 65nm CMOS**

Abdel Martinez Alonso, Masaya Miyahara, Akira Matsuzawa

*Tokyo Institute of Technology, Japan*

## Tuesday, September 12

### Digital Processors

Session Code: A6L-E  
 Location: AV03.12  
 Time: 16:40 - 17:40  
 Chair(s): Sylvain Clerc; *STMicroelectronics*  
 Stefan Rusu; *TSMC*

- 16:40 Design Margin Elimination in a Near-Threshold Timing Error Masking-Aware 32-Bit ARM Cortex M0 in 40nm CMOS**  
 Hans Reyserhove, Wim Dehaene  
*KU Leuven, Belgium*
- 17:00 A 2.7pJ/Cycle 16MHz SoC with 4.3nW Power-Off ARM Cortex-M0+ Core in 28nm FD-SOI**  
 Guénolé Lallement<sup>3</sup>, Fady Abouzeid<sup>2</sup>, Martin Cochet<sup>3</sup>, Jean-Marc Daveau<sup>2</sup>, Philippe Roche<sup>2</sup>, Jean-Luc Autran<sup>1</sup>  
<sup>1</sup>*Aix Marseille University (IM2NP), France*; <sup>2</sup>*ST Microelectronics, France*; <sup>3</sup>*ST Microelectronics - Aix Marseille University (IM2NP), France*
- 17:20 Near-Vt Adaptive Microprocessor and Power-Management-Unit System Based on Direct Error Regulation**  
 Seongjong Kim, Joao Pedro Cerqueira, Mingoo Seok  
*Columbia University, United States*

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## Wednesday, September 13

### Joint Plenary 3: Hans Stork, ON Semiconductor - Smart Power for Automotives

Session Code: B1L-A  
Location: Vesalius  
Time: 08:45 - 09:25  
Chair(s): Jo De Boeck; *imec*

**09:00 Smart Power for Automotives**  
Johannes Stork  
*ON Semiconductor, United States*

## Wednesday, September 13

### High Speed ADC

Session Code: B2L-B  
 Location: AP00.15  
 Time: 10:10 - 11:50  
 Chair(s): Lucien Breems; *NXP Semiconductors N.V.*  
 Georgi Radulov; *Technische Universiteit Eindhoven*

- 10:10 A 36.4dB SNDR @ 5GHz 1.25GS/s 7b 3.56mW Single-Channel SAR ADC in 28nm Bulk CMOS**  
 Athanasios Ramkaj<sup>1</sup>, Maarten Strackx<sup>2</sup>, Michiel Steyaert<sup>1</sup>, Filip Tavernier<sup>1</sup>  
<sup>1</sup>*KU Leuven, Belgium*; <sup>2</sup>*Nokia, Bell Labs, Belgium*
- 10:30 A 28 nm 2 GS/s 5-b Single-Channel SAR ADC with gm-Boosted StrongARM Comparator**  
 Pierluigi Cenci<sup>2</sup>, Muhammed Bolatkale<sup>3</sup>, Robert Rutten<sup>3</sup>, Gerard Lassche<sup>1</sup>, Kofi Makinwa<sup>2</sup>, Lucien Breems<sup>3</sup>  
<sup>1</sup>*Catena Microelectronics, Netherlands*; <sup>2</sup>*Delft University of Technology, Netherlands*; <sup>3</sup>*NXP Semiconductors, Netherlands*
- 10:50 A 43.6-dB SNDR 1-GS/s Single-Channel SAR ADC Using Coarse and Fine Comparators with Background Comparator Offset Calibration**  
 Guanhua Wang<sup>2</sup>, Kexu Sun<sup>2</sup>, Qing Zhang<sup>1</sup>, Salam Elahmadi<sup>1</sup>, Ping Gui<sup>2</sup>  
<sup>1</sup>*Menara Network, United States*; <sup>2</sup>*Southern Methodist University, United States*
- 11:10 A 12b, 1 GSps TI Pipelined-SAR Converter with 65 dB SFDR Through Buffer Linearization and Gain Mismatch Correction in 28nm FD-SOI**  
 Mattias Palm, Daniele Mastantuono, Roland Strandberg, Lars Sundström, Sven Mattisson  
*Ericsson AB, Sweden*
- 11:30 Background Calibration Using Noisy Reference ADC for a 12b 600MS/s 2xTI SAR ADC in 14nm CMOS FinFET**  
 Danny Luu<sup>1</sup>, Lukas Kull<sup>2</sup>, Thomas Toifl<sup>2</sup>, Christian Menolfi<sup>2</sup>, Matthias Braendli<sup>2</sup>, Pier Andrea Francese<sup>2</sup>, Thomas Morf<sup>2</sup>, Marcel Kossel<sup>2</sup>, Hazar Yueksel<sup>2</sup>, Alessandro Cevrero<sup>2</sup>, Ilter Ozkaya<sup>2</sup>, Qiuting Huang<sup>1</sup>  
<sup>1</sup>*ETH Zurich, Switzerland*; <sup>2</sup>*IBM Research Zurich, Switzerland*

## Wednesday, September 13

### Transmitters and Power Amplifiers for mm-Wave and IoT

Session Code: B2L-C

Location: AV91.12

Time: 10:10 - 12:10

Chair(s): Domine Leenaerts; *NXP Semiconductors N.V.*  
Jussi Ryynanen; *Aalto University*

**10:10 Class-AB and Class-J 22 dBm SiGe HBT PAs for X -Band Radar Systems**

Paolo Scaramuzza<sup>1</sup>, Carlo Rubino<sup>3</sup>, Marc Tiebout<sup>3</sup>, Michele Caruso<sup>3</sup>, Markus Ortner<sup>2</sup>, Andrea Neviani<sup>1</sup>, Andrea Bevilacqua<sup>1</sup>  
<sup>1</sup>DEI, University of Padova, Italy; <sup>2</sup>DICE GmbH, Austria;  
<sup>3</sup>Infineon Technologies Villach, Austria

**10:30 A 13.2-dBm, 138-GHz I/Q RF-DAC with 64-QAM and OFDM Free-Space Constellation Formation**

Stefan Shopov<sup>2</sup>, Ozan Gurbuz<sup>1</sup>, Gabriel Rebeiz<sup>1</sup>, Sorin Voinigescu<sup>2</sup>  
<sup>1</sup>University of California at San Diego, United States; <sup>2</sup>University of Toronto, Canada

**10:50 Single-BAW Multi-Channel Transmitter with Low Power and Fast Start-Up Time**

Phillip Nadeau, Rabia Tugce Yazicigil, Anantha Chandrakasan  
MIT, United States

**11:10 A 15-Bit 28nm CMOS Fully-Integrated 1.6W Digital Power Amplifier for LTE IoT**

Jörg Fuhrmann<sup>3</sup>, José Moreira<sup>1</sup>, Patrick Oßmann<sup>5</sup>, Andreas Springer<sup>5</sup>, Robert Weigel<sup>2</sup>, Harald Pretl<sup>4</sup>  
<sup>1</sup>formerly Intel, Germany; <sup>2</sup>Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; <sup>3</sup>Intel DMCE, Friedrich-Alexander-Universität Erlangen-Nürnberg, Austria; <sup>4</sup>Intel DMCE, Johannes Kepler University of Linz, Austria; <sup>5</sup>Johannes Kepler University of Linz, Austria

**11:30 A 60GHz 8-Way Phased Array Front-End with TR Switching and Calibration-Free beamsteering in 28nm CMOS**

Khaled Khalaf<sup>1</sup>, Kristof Vaesen<sup>1</sup>, Steven Brebels<sup>1</sup>, Giovanni Mangraviti<sup>1</sup>, Michael Libois<sup>1</sup>, Charlotte Soens<sup>1</sup>, Piet Wambacq<sup>2</sup>  
<sup>1</sup>imec, Belgium; <sup>2</sup>imec, VUB, Belgium

**11:50 A 25-Gb/s 60 GHz Digital Power Amplifier in 28nm CMOS**

Kaushik Dasgupta<sup>1</sup>, Saeid Daneshgar<sup>1</sup>, Chintan Thakkar<sup>1</sup>, Kunal Datta<sup>2</sup>, James Jaussi<sup>1</sup>, Bryan Casper<sup>1</sup>  
<sup>1</sup>Intel Corporation, United States; <sup>2</sup>Skyworks Inc., United States

## Wednesday, September 13

### Biomedical Circuits and Systems

Session Code: B2L-D  
 Location: AV01.12  
 Time: 10:10 - 11:50  
 Chair(s): Roland Thewes; *Technische Universität Berlin*  
 Andreas Demosthenous; *University College London*

- 10:10 A Reconfigurable 24 × 40 Element Transceiver ASIC for Compact 3D Medical Ultrasound Probes**  
 Eunuchul Kang<sup>2</sup>, Qing Ding<sup>2</sup>, Maysam Shabanmotlagh<sup>2</sup>, Pieter Kruizinga<sup>1</sup>, Zu-Yao Chang<sup>2</sup>, Emile Noothout<sup>2</sup>, Hendrik Vos<sup>1</sup>, Johan Bosch<sup>1</sup>, Martin Verweij<sup>2</sup>, Nicolaas de Jong<sup>1</sup>, Michiel Pertijs<sup>2</sup>  
<sup>1</sup>Erasmus MC, Netherlands; <sup>2</sup>TU Delft, Netherlands
- 10:30 A Multi-Sensor and Parallel Processing SoC for Wearable and Implantable Telemetry Systems**  
 Philipp Schönle<sup>1</sup>, Giovanni Rovere<sup>1</sup>, Florian Glaser<sup>1</sup>, Jonathan Bösser<sup>1</sup>, Noé Brun<sup>1</sup>, Xu Han<sup>1</sup>, Thomas Burger<sup>1</sup>, Schekeb Fateh<sup>1</sup>, Qing Wang<sup>2</sup>, Luca Benini<sup>1</sup>, Qiuting Huang<sup>1</sup>  
<sup>1</sup>Integrated Systems Laboratory, ETH Zürich, Switzerland;  
<sup>2</sup>Internal Medicine Branch and Division of Nephrology and Hypertension, Department of Medicine, CHUV, Switzerland
- 10:50 0.3V Ultra-Low Power Sensor Interface for EMG**  
 Sirma Orguc, Harneet Singh Khurana, Hae-Seung Lee, Anantha P. Chandrakasan  
 MIT, United States
- 11:10 A 24  $\mu$ W 38.51 m $\Omega$ rms Resolution Bio-Impedance Sensor with Dual Path Instrumentation Amplifier**  
 Kwantae Kim<sup>2</sup>, Kiseok Song<sup>1</sup>, Kyeongryeol Bong<sup>2</sup>, Jaehyuk Lee<sup>2</sup>, Kwonjoon Lee<sup>1</sup>, Yongsu Lee<sup>2</sup>, Unsoo Ha<sup>2</sup>, Hoi-Jun Yoo<sup>2</sup>  
<sup>1</sup>Healthrian, Korea; <sup>2</sup>KAIST, Korea
- 11:30 A CMOS Current Driver with Built-in Common Mode Signal Reduction Capability for EIT**  
 Yu Wu<sup>2</sup>, Dai Jiang<sup>2</sup>, Peter Langlois<sup>2</sup>, Richard Bayford<sup>1</sup>, Andreas Demosthenous<sup>2</sup>  
<sup>1</sup>Middlesex University London, United Kingdom; <sup>2</sup>University College London, United Kingdom

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## Wednesday, September 13

### ESSCIRC Keynote 2: Sven Mattisson, Ericsson - Overview of 5G Requirements & Future Wireless Networks

Session Code: B3L-B  
Location: AP00.15  
Time: 13:30 - 14:10  
Chair(s): Filip Tavernier; *KU Leuven*

**13:30 Overview of 5G Requirements and Future Wireless Networks**

Sven Mattisson  
*Ericsson Research, Sweden*

## Wednesday, September 13

### High Efficiency ADC

Session Code: B4L-B

Location: AP00.15

Time: 14:20 - 15:20

Chair(s): Dieter Draxelmayr; *Infineon Technologies AG*  
Andrea Baschiroto; *Università degli Studi di Milano-Bicocca*

- 14:20 A 10b 20MS/s SAR ADC with a Low-Power and Area-Efficient DAC-Compensated Reference**  
Maoqiang Liu, Arthur van Roermund, Pieter Harpe  
*Eindhoven University of Technology, Netherlands*
- 14:40 An Energy Reduced Sampling Technique Applied to a 10b 1MS/s SAR ADC**  
Harijot Singh Bindra<sup>2</sup>, Anne-Johan Annema<sup>2</sup>, Simon M. Louwsma<sup>1</sup>, Ed J.M. van Tuijl<sup>1</sup>, Bram Nauta<sup>2</sup>  
<sup>1</sup>*Teledyne DALSA, Netherlands*; <sup>2</sup>*University of Twente, Netherlands*
- 15:00 A Missing-Code-Detection Gain Error Calibration Achieving 63dB SNR for an 11-Bit ADC**  
Guan-Cheng Wang, Yan Zhu, Chi-Hang Chan, Seng-Pan U, Rui Paulo Martins  
*State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, Macau*

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## Wednesday, September 13

### 5G and mm-Wave Frequency Synthesis

Session Code: B4L-C

Location: AV91.12

Time: 14:20 - 15:20

Chair(s): Baudouin Martineau; *Commissariat à l'Energie Atomique et aux Energies Alternatives*  
Alexandre Siligaris; *Commissariat à l'Energie Atomique et aux Energies Alternatives*

- 14:20 A 54-64.8 GHz Subharmonically Injection-Locked Frequency Synthesizer with Transmitter EVM Between -26.5 dB and -28.8 dB in 28 nm CMOS**  
Cheng-Hsueh Tsai, Giovanni Mangraviti, Qixian Shi, Khaled Khalaf, André Bourdoux, Piet Wambacq  
*imec, Belgium*
- 14:40 A 491.52 MHz 840 uW Crystal Oscillator in 28 nm FD-SOI CMOS for 5G Applications**  
Christian Elgaard, Lars Sundström  
*Ericsson Research, Sweden*
- 15:00 A 16-20 GHz LO System with 115 fs Jitter for 24-30 GHz 5G in 28 nm FD-SOI CMOS**  
Staffan Ek, Tony Pålsson, Anders Carlsson, Andreas Axhult, Anna-Karin Stenman, Henrik Sjöland  
*Ericsson AB, Sweden*

## Wednesday, September 13

### Machine Learning and Neuromorphic Computing

Session Code: B4L-D

Location: AV01.12

Time: 14:20 - 15:40

Chair(s): Shidhartha Das; *ARM Holdings plc*  
Praveen Raghavan; *imec*

**14:20 An Ultra-Low-Power and Mixed-Mode Event-Driven Face Detection SoC for Always-on Mobile Applications**

Changhyeon Kim, Kyeongryeol Bong, Injoon Hong, Kyuho Lee, Sunpill Choi, Hoi-Jun Yoo  
*Korea Advanced Institute of Science and Technology (KAIST), Korea*

**14:40 OCEAN: An on-Chip Incremental-Learning Enhanced Processor with Gated Recurrent Neural Network Accelerators**

Chixiao Chen<sup>1</sup>, Hongwei Ding<sup>2</sup>, Huwan Peng<sup>2</sup>, Haozhe Zhu<sup>1</sup>, Rui Ma<sup>1</sup>, Peiyong Zhang<sup>3</sup>, Xiaolang Yan<sup>3</sup>, Yu Wang<sup>1</sup>, Mingyu Wang<sup>1</sup>, Hao Min<sup>1</sup>, Richard C-J. Shi<sup>1</sup>  
<sup>1</sup>*Fudan University, China*; <sup>2</sup>*University of Washington, United States*; <sup>3</sup>*Zhejiang University, China*

**15:00 A 19.4 nJ/Decision 364K Decisions/s In-Memory Random Forest Classifier in 6T SRAM Array**

Mingu Kang, Sujan Gonugondla, Naresh Shanbhag  
*UIUC, United States*

**15:20 A Highly Accurate Spike Sorting Processor With Reconfigurable Embedded Frames for Unsupervised and Adaptive Analysis of Neural Signals**

Majid Zamani, Dai Jiang, Andreas Demosthenous  
*UCL, United Kingdom*

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## Wednesday, September 13

### Linear Regulators

Session Code: B4L-E  
Location: AV03.12  
Time: 14:20 - 15:20  
Chair(s): Christoph Sandner; *Infineon Technologies AG*  
Drago Strle; *University of Ljubljana*

**14:20 A Synthesizable Time-Based LDO Using Digital Standard Cells and Analog Pass Transistor**

Ahmed Fahmy, Jun Liu, Pavan Terdal, Ryan Madler, Rizwan Bashirullah, Nima Maghari  
*University of Florida, United States*

**14:40 A Digitally Controlled Linear Regulator for Per-Core Wide-Range DVFS of Atom™ Cores in 14nm Tri-Gate CMOS Featuring Non-Linear Control, Adaptive Gain and Code Roaming**

Ramnarayanan Muthukaruppan, Tarun Mahajan, Harish Krishnamurthy, Sumedha Mangal, Am Dhanashekar, Rupak Ghayal, Vivek De  
*Intel Corporation, United States; Intel Corporation, India*

**15:00 A Sub-100nW Power Supply Unit Embedding Untrimmed Timing and Voltage References for Duty-Cycled uW-Range Load in FDSOI 28nm**

Anthony Quelen, Franck Badets, Gael Pillonnet  
*CEA-LETI, France*

## Thursday, September 14

### Joint Plenary 4: Tetsuo Endoh, Tohoku University - Spintronics Applications: STT-MRAM and Non Volatile Logic

Session Code: C1L-A  
Location: Vesalius  
Time: 09:00 - 09:40  
Chair(s): Jo De Boeck; *imec*

**08:45 Spintronics applications: STT-MRAM and Non Volatile  
Logic**  
Tetsuo Endoh  
*Tohoku University, Japan*

## Thursday, September 14

### Power Management and Harvesting

Session Code: C2L-B

Location: AP00.15

Time: 10:20 - 12:00

Chair(s): Bernard Wicht; *Hochschule Reutlingen*  
Ravi Karadi; *NXP Semiconductors N.V.*

- 10:20 Switched Capacitor DC-DC Converter with Switch Conductance Modulation and Pseudo-Fixed Frequency Control**  
Dennis Larsen<sup>3</sup>, Martin Vinter<sup>2</sup>, Ivan Jørgensen<sup>1</sup>  
<sup>1</sup>DTU, Denmark; <sup>2</sup>GN Hearing, Denmark; <sup>3</sup>GN Hearing & DTU, Denmark
- 10:40 Unsymmetrical Parallel Switched-Capacitor (UP-SC) Regulator with Fast Searching Optimum Ratio Technique**  
Yen-Ting Lin<sup>1</sup>, Wen-Hau Yang<sup>1</sup>, Yu-Sheng Ma<sup>1</sup>, Yan-Jiun Lai<sup>1</sup>, Hung-Wei Chen<sup>1</sup>, Ke-Horng Chen<sup>1</sup>, Chin-Long Wey<sup>1</sup>, Ying-Hsi Lin<sup>2</sup>, Jian-Ru Lin<sup>2</sup>, Tsung-Yen Tsai<sup>2</sup>  
<sup>1</sup>National Chiao Tung University, Taiwan; <sup>2</sup>Realtek Semiconductor Corp, Taiwan
- 11:00 A 100-mW Fully Integrated DC-DC Converter with Double Galvanic Isolation**  
Nunzio Greco<sup>1</sup>, Alessandro Parisi<sup>1</sup>, Pierpaolo Lombardo<sup>1</sup>, Nunzio Spina<sup>2</sup>, Egidio Ragonese<sup>2</sup>, Giuseppe Palmisano<sup>1</sup>  
<sup>1</sup>DIEEI, Università degli Studi di Catania, Italy;  
<sup>2</sup>STMicroelectronics, Catania, Italy
- 11:20 Wide-Input-Voltage-Range and High-Efficiency Energy Harvester with a 155-mV Startup Voltage for Solar Power**  
Hung-Hsien Wu, Liang-Yun Chen, Chia-Ling Wei  
*National Cheng Kung University, Taiwan*
- 11:40 A 900 MHz RF Energy Harvesting System in 40 nm CMOS Technology with Efficiency Peaking at 47% and Higher Than 30% Over a 22dB Wide Input Power Range**  
Jialue Wang<sup>3</sup>, Yang Jiang<sup>1</sup>, Johan Dijkhuis<sup>4</sup>, Guido Dolmans<sup>5</sup>, Gao Hao<sup>2</sup>, Peter Baltus<sup>2</sup>  
<sup>1</sup>Delft University of Technology / imec-NL, Netherlands;  
<sup>2</sup>Eindhoven University of Technology, Netherlands; <sup>3</sup>Eindhoven University of Technology / imec-NL, Netherlands; <sup>4</sup>imec-NL, Netherlands; <sup>5</sup>imec-NL / Eindhoven University of Technology, Netherlands

## Thursday, September 14

### Embedded Memories

Session Code: C2L-C

Location: AV91.12

Time: 10:20 - 12:00

Chair(s): Tobias Gemmeke; imec  
Atila Alvandpour; Linköping University

**10:20 A System of Array Families and Synthesized Soft Arrays for the POWER9™ Processor in 14nm SOI FinFET Technology**

Philipp Salz, Albert Frisch, Wolfgang Penth, Jens Noack, Thomas Kalla, Rolf Sautter, Michael Kugel, Otto Andreas Torreyter, Gordon Sapp, Michael Lee, Eric Fluhr, Amira Rozenfeld, Juergen Pille, Dieter Wendel  
*IBM Systems, Israel; IBM Systems, United States; IBM Systems, Germany*

**10:40 An 800Mhz Mixed-VT 4T Gain-Cell Embedded DRAM in 28nm CMOS Bulk Process for Approximate Computing Applications**

Robert Giterman<sup>1</sup>, Alexander Fish<sup>1</sup>, Narkis Geuli<sup>3</sup>, Elad Mentovich<sup>3</sup>, Andreas Burg<sup>2</sup>, Adam Teman<sup>1</sup>  
*<sup>1</sup>Bar-Ilan University, Israel; <sup>2</sup>EPFL, Switzerland; <sup>3</sup>Mellanox Technologies, Israel*

**11:00 An 80-MHz 0.4V ULV SRAM Macro in 28nm FDSOI Achieving 28-fJ/Bit Access Energy with a ULP bitcell and on-Chip Adaptive Back Bias Generation**

Thomas Haine, Quoc-Khoi Nguyen, François Stas, Ludovic Moreau, Denis Flandre, David Bol  
*Université catholique de Louvain, Belgium*

**11:20 1.56GHz/0.9V Energy-Efficient Reconfigurable CAM/SRAM Using 6T-CMOS bitcell**

Navneet Gupta<sup>3</sup>, Adam Makosiej<sup>1</sup>, Andrei Vladimirescu<sup>2</sup>, Amara Amara<sup>2</sup>, Costin Anghel<sup>2</sup>  
*<sup>1</sup>Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA-LETI), France; <sup>2</sup>ISEP, France; <sup>3</sup>ISEP and CEA LETI, France*

**11:40 A 32KB 18ns Random Access Time Embedded PCM with Enhanced Program Throughput for Automotive and Smart Power Applications**

Marco Pasotti<sup>1</sup>, Marcella Carissimi<sup>1</sup>, Chantal Auricchio<sup>1</sup>, Donatella Brambilla<sup>1</sup>, Emanuela Calvetti<sup>1</sup>, Laura Capecchi<sup>1</sup>, Luigi Croce<sup>1</sup>, Daniele Gallinari<sup>1</sup>, Cristina Mazzaglia<sup>1</sup>, Vikas Rana<sup>1</sup>, Riccardo Zurla<sup>2</sup>, Alessandro Cabrini<sup>2</sup>, Guido Torelli<sup>2</sup>  
*<sup>1</sup>STMicroelectronics, Italy; <sup>2</sup>STMicroelectronics, India; <sup>2</sup>University of Pavia, Italy*

## Thursday, September 14

### Wireless SOC

Session Code: C2L-D

Location: AV01.12

Time: 10:20 - 12:00

Chair(s): Marc Borremans; *Huawei*  
Giuseppe Gramegna; *Huawei Technologies*

**10:20 A 2x14bit Digital Transmitter with Memoryless Current Unit Cells and Integrated AM/PM Calibration**

Mark Ingels, Davide Dermit, Yao Liu, Hans Cappelle, Jan Craninckx  
*imec, Belgium*

**10:40 A Low Voltage 0.8V RF Receiver in 28nm CMOS for 5GHz WLAN**

Atsushi Shirane, Shusuke Kawai, Hiromitsu Aoyama, Rui Ito, Toshiya Mitomo, Hiroyuki Kobayashi, Hiroshi Yoshida, Hideaki Majima, Ryuichi Fujimoto, Hiroshi Tsurumi  
*Toshiba Corporation, Japan*

**11:00 A 65nm CMOS 2x2 MIMO Multi-Band LTE RF Transceiver for Small Cell Base Stations**

Kyoohyun Lim, Sanghoon Lee, Byeongmoo Moon, Hwahyeong Shin, Kisub Kang, Yongha Lee, Seungbeom Kim, Jinhyeok Lee, Hyungsuk Lee, Hyunchul Shim, Cheolhoon Sung, Geumyoung Park, Garam Lee, Minjung Kim, Seokyoung Park, Hyosun Jung, Jongryul Lee  
*FCI, Korea*

**11:20 A Low-Noise Reconfigurable Full-Duplex Front-End with Self- Interference Cancellation and Harmonic-Rejection Power Amplifier for Low Power Radio Applications**

Tong Zhang, Yongdong Chen, Chenxi Huang, Jacques Rudell  
*University of Washington, United States*

**11:40 A SAW-Less RF-SoC for Cellular IoT Supporting EC-GSM-IoT -121.7 dBm Sensitivity Through EGPRS2A 592 kbps Throughput**

Benjamin Weber<sup>2</sup>, Matthias Korb<sup>2</sup>, David Tschopp<sup>1</sup>, Stefan Altorfer<sup>1</sup>, Jürgen Rogin<sup>1</sup>, Harald Kröll<sup>2</sup>, Qiuting Huang<sup>2</sup>  
<sup>1</sup>Advanced Circuit Pursuit (ACP), Switzerland; <sup>2</sup>ETH Zurich, Switzerland

## Thursday, September 14

### **ESSCIRC Keynote 3: Harish Krishnaswamy, Columbia Univ. - Integrated Antenna-Interface Components**

Session Code: C3L-B

Location: AP00.15

Time: 13:30 - 14:10

Chair(s): Patrick Reynaert; *KU Leuven*

#### **13:30 Integrated Antenna-Interface Components – A Blessing for Wireless Transceivers**

Harish Krishnaswamy

*University of Columbia, United States*

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## Thursday, September 14

### DC-DC Converters

Session Code: C4L-B  
Location: AP00.15  
Time: 14:20 - 15:20  
Chair(s): Johan Janssens; *ON Semiconductor*  
Michiel Steyaert; *KU Leuven*

- 14:20 A 92.2% Peak-Efficiency Self-Resonant Hybrid Switched-Capacitor LED Driver in 0.18 $\mu$ m CMOS**  
Juan C Castellanos, Mert Turhan, Marcel A.M. Hendrix, Arthur van Roermund, Eugenio Cantatore  
*Eindhoven University of Technology, Netherlands*
- 14:40 A 12-48V Wide-Vin 9-15MHz Soft-Switching Controlled Resonant DCDC Converter**  
Juergen Wittmann<sup>2</sup>, Tobias Funk<sup>2</sup>, Thoralf Rosahl<sup>3</sup>, Bernhard Wicht<sup>1</sup>  
*<sup>1</sup>Leibniz University Hannover, Germany; <sup>2</sup>Reutlingen University, Germany; <sup>3</sup>Robert Bosch GmbH, Reutlingen, Germany*
- 15:00 A Low Quiescent Current and Cross Regulation Single-Inductor Dual-Output Converter with Stacking MOSFET Driving Technique**  
Yu-Sheng Ma<sup>1</sup>, Wen-Hau Yang<sup>1</sup>, Yen-Ting Lin<sup>1</sup>, Hsin Chen<sup>1</sup>, Li-Chi Lin<sup>1</sup>, Ke-Horng Chen<sup>1</sup>, Chin-Long Wey<sup>1</sup>, Ying-Hsi Lin<sup>2</sup>, Jian-Ru Lin<sup>2</sup>, Tsung-Yen Tsai<sup>2</sup>, Jui-Lung Chen<sup>3</sup>  
*<sup>1</sup>National Chiao Tung University, Taiwan; <sup>2</sup>Realtek Semiconductor Corp., Taiwan; <sup>3</sup>Vanguard International Semiconductor Corp., Taiwan*

## Thursday, September 14

### Sensor Interfaces

Session Code: C4L-C

Location: AV91.12

Time: 14:20 - 15:40

Chair(s): Hanspeter Schmid; *Fachhochschule Nordwestschweiz*  
Michael Mark; *Infineon Technologies AG*

- 14:20 A 1.85 fA/sqrt(Hz) Fully Integrated Current Read-Out Interface for Sub-pA Current Sensing Applications**  
 Mohammad Amayreh<sup>2</sup>, Matthias Keller<sup>1</sup>, Yiannos Manoli<sup>1</sup>  
<sup>1</sup>*University of Freiburg, Germany*; <sup>2</sup>*Universtiy of freiburg, Germany*
- 14:40 Integrated Hall-Based Magnetic Platform for Position Sensing**  
 Sebastien Leroy, Stefan Rigert, Arnaud Laville, Andrea Ajbl, Gael Close  
*Melexis, Switzerland*
- 15:00 A 5.5 nW Battery-Powered Wireless Ion Sensing System**  
 Hui Wang, Xiaoyang Wang, Jiwoong Park, Abbas Barfidokht, Joseph Wang, Patrick Mercier  
*University of California, San Diego, United States*
- 15:20 A 64×64 High-Density Redox Amplified Coulostatic Discharge-Based Biosensor Array in 180nm CMOS**  
 Alexander Sun, Enrique Alvarez-Fontecilla, A. G. Venkatesh, Eliah Aronoff-Spencer, Drew A. Hall  
*UCSD, United States*

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## Thursday, September 14

### Low Power Radios

Session Code: C4L-D

Location: AV01.12

Time: 14:20 - 15:20

Chair(s): Andrea Mazzanti; *Università degli studi di Pavia*  
Dominique Morche; *Commissariat à l'Energie Atomique  
et aux Energies Alternatives*

**14:20 Isolator-Less Near-Field RFID Reader for Sub-Cranial Powering/Data Link of mm-Sized Implants**

Christopher Sutardja, Jan Rabaey  
*University of California, Berkeley, United States*

**14:40 A 8mW-RX/113mW-TX, Sub-GHz SoC with Time-Dithered PA Ramping for LPWAN Applications**

Hasan Gul<sup>2</sup>, Jac Romme<sup>2</sup>, Paul Mateman<sup>2</sup>, Johan Dijkhuis<sup>2</sup>,  
Xiongchuan Huang<sup>1</sup>, Cui Zhou<sup>2</sup>, Benjamin Busze<sup>2</sup>, Gert-Jan  
van Schaik<sup>2</sup>, Elbert Bechthum<sup>2</sup>, Ming Ding<sup>2</sup>, Arjan Breeschoten<sup>2</sup>,  
Yao-Hong Liu<sup>2</sup>, Christian Bachmann<sup>2</sup>, Guido Dolmans<sup>2</sup>,  
Kathleen Philips<sup>2</sup>

<sup>1</sup>Broadcom, United States; <sup>2</sup>Holst-centre/Imec, Netherlands

**15:00 A Low-Power Compact IEEE 802.15.6 Compatible Human Body Communication Transceiver with Digital Sigma-Delta IIR Mask Shaping**

Bo Zhao<sup>1</sup>, Yong Lian<sup>3</sup>, Ali M. Niknejad<sup>1</sup>, Chun Huat Heng<sup>2</sup>

<sup>1</sup>Berkeley Wireless Research Center (BWRC), United States;

<sup>2</sup>National University of Singapore, Singapore; <sup>3</sup>York University,  
Canada

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