

CONNECT Open Day 2017 Workshop

Leuven, Belgium - 11th September 2017

Abstract

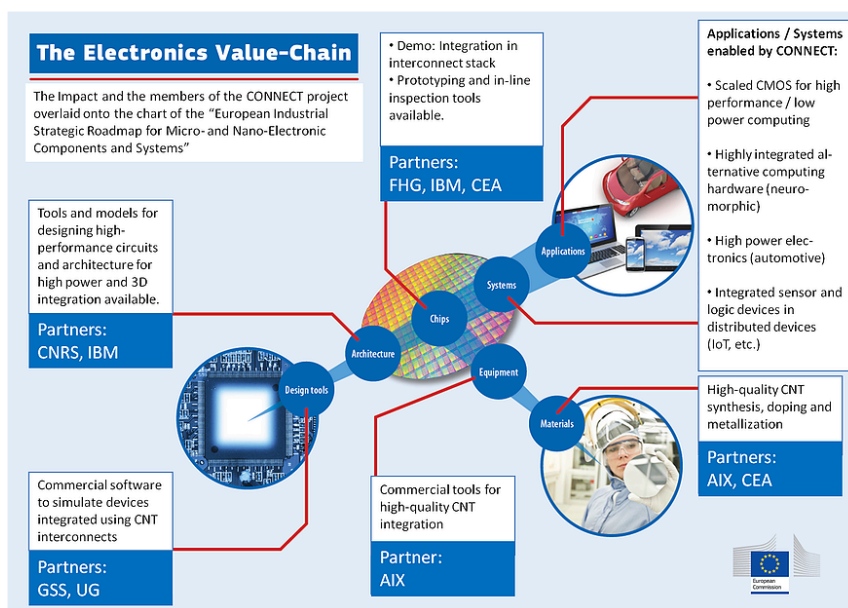
The workshop will provide technical information about emerging interconnect technologies, with the focus on Carbon Nanotubes (CNT). A broad overview of all the major aspects of CNT interconnects will be offered, ranging from the innovative growth/deposition techniques of local and global lines to the novel measurement and simulation methodologies developed to characterize CNT performances. The core of the workshop will be based on the latest results arising from the research within the H2020 EU-funded project CONNECT. Invited talks from academia, research centers and industry will enrich the global perspective of the workshop.

Target Audience

The target audience is students, researchers, engineers and entrepreneurs who have an interest or work in the areas related to advanced and future interconnects for integrated circuits. Since interconnects delay is a major limitation to circuits performance, anyone interested in advanced CMOS technologies will benefit from the topics addressed by the workshops' talks. Researchers working in the field of Carbon Nanotubes, even if not for with direct application in interconnects technology, will also find cross-disciplinary interest in this workshop. Finally, CMOS circuit designers will be able to gather useful information on modeling, design and optimization opportunities offered by Carbon Nanotubes based technologies.

Registration Fee

Thanks to the contribution of the EU Community through the project CONNECT, the regular registration fee of 60€ will be waived for the first 50 attendees who register to this workshop (*).

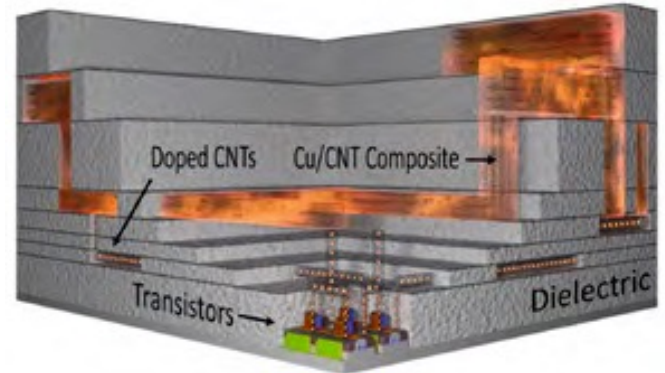


(*) Offer is valid only on regular registration fee for those who attend also the full ESSDERC/ESSCIRC conference. The offer is not valid for those who decide to attend the Workshop only. Registration fee will be, in this case, 150€.



Background on CONNECT Project CarbON Nanotube compositE InterconneCTs

As the chip size goes down, interconnects become major bottlenecks irrespective of the application domain due to electromigration issues and an ever-increasing power consumption. The CONNECT project investigates ultra-fine CNT lines and metal- CNT composite material for addressing the issues of current state-of-the-art copper interconnects. Novel CNT interconnect architectures for the exploration of circuit- and architecture-level performance and energy efficiency will be developed. CMOS compatibility as well as challenges of transferring new processes into industrial mass production will be addressed. The members of the CONNECT consortium from Germany, Switzerland, Great Britain and France are embedded along the electronics value chain from fundamental research to end- users and bring together some of the most renowned research groups in that field in Europe. With significantly improved electrical resistivity, ampacity, thermal and electromigration properties of CNT interconnects compared to state-of-the-art approaches for conventional copper interconnects, an increased power and scaling density of CMOS or CMOS extension will be available and applicable to



alternative computing schemes such as neuromorphic computing.

The technologies developed in this project are key for both performance and manufacturability of scaled microelectronics to manifest miniaturized microelectronic products with enhanced functionality at ever decreasing cost. The procurement of CONNECT will foster the recovery of market shares of the European electronic sector and prepare the industry for future developments of the electronic landscape.

You can find more information about CONNECT project at the website
www.connect-h2020.eu



CONNECT Open Day 2017 Workshop Agenda

Date: 11th September 2017

Venue: TBC

11 th September 2017		
8.00	Arrival & Registration	
8.30	Welcome and CONNECT Open Day Introduction	Prof. Aida Todri-Sanial Dr. Salvatore M. Amoroso (Organizers)
8.45	Overview of the EC H2020 CONNECT project	Dr. Benjamin Uhlig (Fraunhofer-Dresden)
9.00	Highly Energy-Efficient Digital NanoSystems: New Logic, Memory, Interconnects, & 3D integration	Dr. Gage Krieger Hills (Stanford University)
9.35	Direct, dry deposition of high quality SWNT thin films	Prof. Esko Kauppinen (Aalto University)
10.10	Coffee Break	
10.40	Doped CNTs for advanced local interconnects	Dr. Jean Dijon (CEA-Grenoble)
11.15	CNT-metal-composites for global interconnects	Dr. Benjamin Uhlig (Fraunhofer-Dresden)
11.50	Vertical Multi-walled CNT interconnects evaluation at full wafer level	Dr. Marleen van der Veen (IMEC)
12.30	Lunch Break	
14.00	Heterogeneous integration of low-dimensional nanomaterials	Dr. Shu-Jen Han (IBM TJ Watson)
14.35	Manufacturability of CNT interconnects	Dr. Bingan Chen (AIXTRON-UK)
15.10	Coffee Break	
15.40	Thermal and Electrical Characterization of CNTs interconnects	Dr. Bernd Gotsmann (IBM-Zurich)
16.15	Hierarchical multi-physics simulation of CNT interconnects	Prof. Aida Todri-Sanial (CNRS-Montpellier)
16.50	Wrap Up & Closure	